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Electromigration Enhanced Kinetics of Cu-Sn Intermetallic Compounds in Pb Free Solder Joints and Cu Low-k Dual Damascene Processing Using Step and Flash Imprint Lithography

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by

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Dedication

To my dear parents, family, and friends

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This dissertation constitutes two major sections. In the first major section, a kinetic analysis was established to investigate the electromigration (EM), enhanced intermetallic compound (IMC) growth and void formation for Sn-based Pb-free solder joints to Cu under bump metallization (UBM). The model takes into account the interfacial intermetallic reaction, Cu-Sn interdiffusion, and current stressing. A new approach was developed to derive atomic diffusivities and effective charge numbers based on Simulated Annealing (SA) in conjunction with the kinetic model. The finite difference (FD) kinetic model based on this approach accurately predicted the intermetallic compound growth when compared to empirical observation. The ultimate electromigration failure of the solder joints was caused by extensive void formation at the intermetallic interface. The void formation mechanism was analyzed by modeling the

vacancy transport under electromigration. The effects of current density and Cu diffusivity in Sn solder were also investigated with the kinetic model.

The second major section describes the integration of Step and Flash Imprint Lithography (S-FIL®) into an industry standard Cu/low-k dual damascene process. The yield on a Back End Of the Line (BEOL) test vehicle that contains standard test structures such as via chains with 120 nm vias was established by electrical tests. S-FIL shows promise as a cost effective solution to patterning sub 45 nm features and is capable of simultaneously patterning two levels of interconnect structures, which provides a low cost BEOL process. The critical processing step in the integration is the reactive ion etching (RIE) process that transfers the multilevel patterns to the inter-level dielectrics (ILD). An *in-situ*, multistep etch process was developed that gives excellent pattern structures in two industry standard Chemical Vapor Deposited (CVD) low-k dielectrics. The etch process showed excellent pattern fidelity and a wide process window. Electrical testing was conducted on the test vehicle to show that this process renders high yield and consistent via resistance. Discussions of the failure behaviors that are characteristic to the use of S-FIL are provided.

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MAJOR SECTION I

ELECTROMIGRATION ENHANCED KINETICS OF CU-SN INTERMETALLIC COMPOUNDS IN PB FREE SOLDER JOINTS

Chapter 1: Introduction

The advent of information technologies has heralded pervasive transformations to the cultures and economy of the contemporary world. The progression of the digital era is propelled by the technology innovations from the microelectronic industry that have enabled instantaneous and almost ubiquitous flow and exchange of information. This dissertation focuses on two major sections which found their applications in two critical areas of active research of the microelectronic industry: electronic packaging reliability and emerging lithography.

Electronic packaging reliability

The first major section, Chapters 1 through 6, describes a study of the electromigration (EM) reliability of advanced flip-chip packaging using lead free solders. In order to achieve the higher packing density that is required to meet the Moore's law, packaging technology is shifting from peripheral wire bonding to area array flip chip packaging. In addition, there is an escalating demand to replace all lead bearing solder materials because of environmental concerns. Driven by the global initiative to minimize the use of hazardous substances, the microelectronic industry is eliminating the use of lead in the soldering metallurgy. Therefore, there is tremendous interest in the research related to lead-free, flip chip packaging because it is an eco-friendly assembly process that meets the requirements for both electrical performance and environmental standards.

Nevertheless, a myriad of reliability concerns have arisen when the lead-free solder materials are implemented in commercial products. Among them, electromigration poses the most pressing challenge because of the demand for increasing current density and smaller solder bump size.

Intensive investigation has been carried out to study electromigration in fine conductor lines in multilevel interconnect structures since it was found to cause failures of aluminum lines in integrated circuits [1.1]. For packaging level reliability, the failure mechanism induced by electromigration in solder bumps was found to be very different from the interconnect electromigration failures [1.2, 1.3]. During the solder reflow process, intermetallic compounds (IMC) form extensively between the solder materials and the under-bump metallization (UBM). These intermetallic compounds provide mechanical bonding between the solder material and the silicon chip. However, they also substantially complicate the electromigration phenomenon and change the damage formation mechanisms. This is because electromigration, intermetallic compound growth, and chemical diffusion all take place simultaneously during current stressing.

Major Section I of this dissertation focuses on two objectives. First, a kinetic model was established that solves the growth of the intermetallic compounds by taking into account the mass transport induced by electromigration and chemical diffusion. Vacancy transport, which plays a critical role in controlling void formation, was also calculated with this model. These analyses improved understanding of intermetallic compound kinetics and void formation under electromigration. Second, lack of the pertinent material parameters was recognized by Orchard and Greer [1.4] as the major hindrance to quantitative verification of the analysis for intermetallic compound kinetics and solder reliability. By fitting experimental data [1.5, 1.6] to the kinetic model using

the simulated annealing (SA) technique, these important parameters, diffusion coefficients and effective charge numbers, were obtained.

Emerging lithography

The second major section, Chapters 7 through 13, focuses on the integration of Step and Flash Imprint Lithography (S-FIL) into Cu/low-k Back End Of the Line (BEOL) dual damascene processing. Microlithography has been the enabling technology that drives the continuous miniaturization of transistors and provides ever increasing speed and density in advanced integrated circuits (ICs). However, major technology barriers are encountered at sub 32 nm imaging, including soaring cost, poor photoresist performance, and delay in development of a high resolution exposure tool. Step and Flash Imprint Lithography (S-FIL) is considered one of the most promising candidates for next-generation lithography (NGL) due to its high resolution and very competitive cost of ownership (CoO).

The state of the art Back End Of the Line process employs Cu interconnects and a low dielectric constant (low k) inter-level dielectric (ILD) to reduce signal delay, cross talk, and power dissipation. These Cu interconnects are made by the "dual damascene process" and comprise the via and the line structures. The conventional dual damascene processing requires separate lithography and etching steps to pattern the vias and the lines prior to the subsequent metallization and chemical mechanical polishing (CMP) steps that complete each of the wiring levels. The process has become increasingly complex and expensive because as many as ten or more wiring levels are needed in advanced chip designs.

S-FIL in conjunction with a multilevel template is demonstrated in this study to provide a new and viable approach to dual damascene processing, which significantly

reduces the number of steps required to build the interconnect structures and thereby lower the wafer processing cost. Intensive studies focused on development of the multilevel pattern transfer etching technique and the process integration with dual damascene process flow is reported. Electrical testing was conducted on a 120 nm node test vehicle and these data proved viability of this processing approach.

1.1 FLIP CHIP TECHNOLOGY

The device scaling of microelectronics packs more and more computing power into one single micro-chip. This requires increasing I/O (input and output) density in order to facilitate the exchange of information between the chip and the outside world. Originally developed by IBM in the 1960s to be used in their mainframe systems [1.7], flip chip technology substantially outstrips conventional wire bonding in I/O density and bus speed. The smaller form factor of flip chip packaging is also very attractive for new applications in mobile devices.

Flip chip technology, also named by IBM as controlled collapse chip connection (C4), utilizes solder bumps deposited on the under-bump metallization on the chip to connect to the top surface metallurgy (TSM) on the substrate [1.8]. Because the bump array can occupy the entire chip area, the I/O density is significantly increased. Figure 1.1 shows one of the typical packing options in which flip chip solder bumps are used to connect the silicon chip to the carrier substrate. Ball grid array (BGA) is used to connect the carrier substrate to the printed circuit board (PCB).

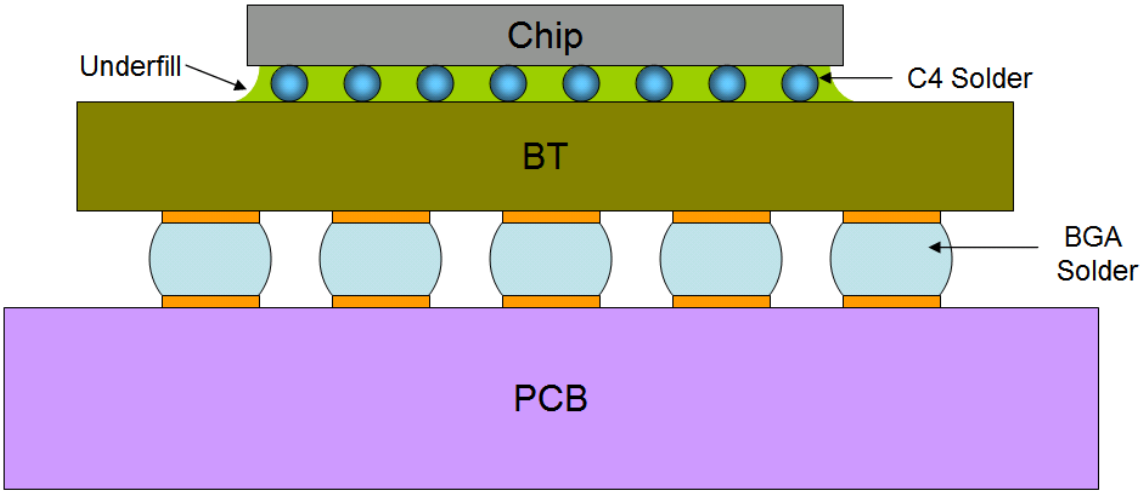


Figure 1.1: Schematic diagram showing a cross section of the flip chip solder bumps on a BT (bismaleimide triazine) substrate and the plastic ball grid array (PBGA) on a printed circuit board (PCB) (Source: S. K. Kang *et al*. in Ref [1.9]; this diagram was redrawn by the author)

Figure 1.2 describes the typical process sequence of flip chip packaging. The first step is the wafer bumping process to form the under-bump metallization and deposit the solder bump alloy at the bump pad area, as shown in Figure 1.2 (a). Photolithography with a thick resist layer is used to define the bump site. The under-bump metallization, such as nickel or copper, is electroplated into the bump pattern, and the solder is subsequently electroplated on top of the under-bump metallization. The under-bump metallization needs to provide several functions such as solder wetability, good adhesion, and adequate electrical conductivity. After electroplating, the photoresist is stripped and the field metal outside the bump site is removed by wet etching. Figure 1.3 shows a diagram of a solder bump stud after completion of the wafer bumping process.

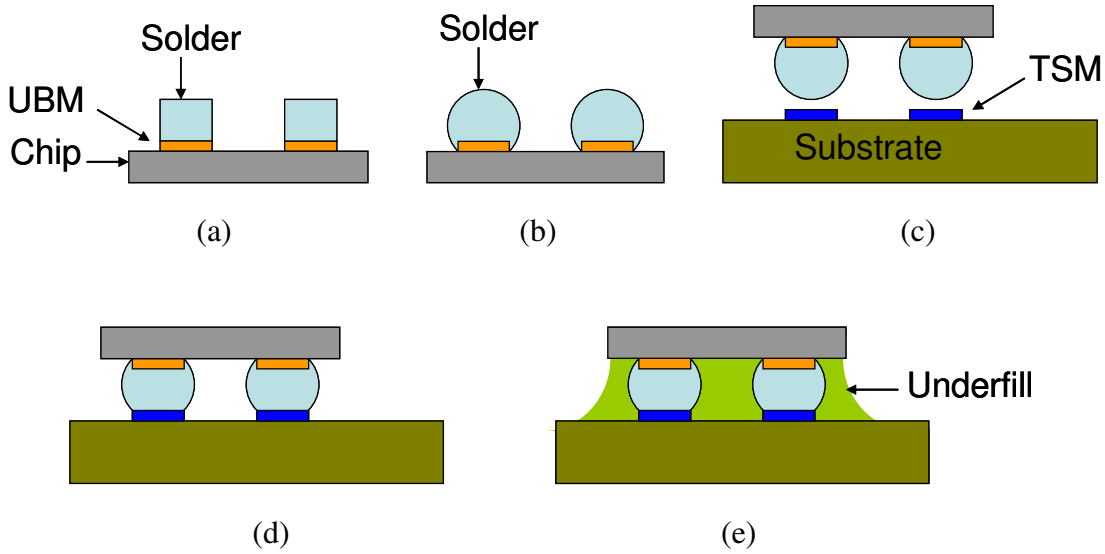


Figure 1.2: Flip-chip process sequence on solder-based bumps: (a) bumping, (b) solder reflow, (c) alignment, (d) solder reflow, and (e) underfilling and curing

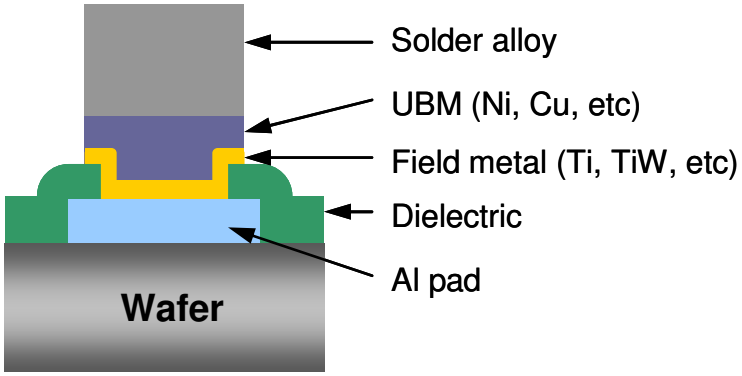


Figure 1.3: Diagram of a solder bump stack after wafer bumping process

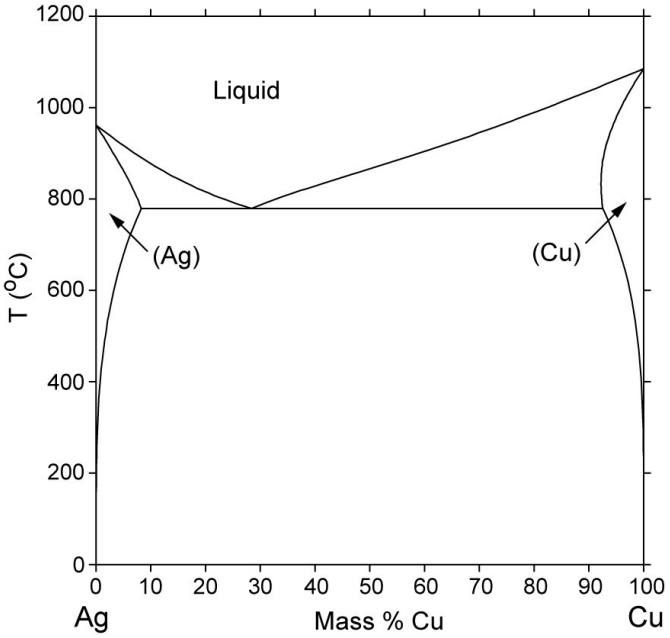
Once bumping is completed, the wafer is heated to reflow the solder bumps, as shown in Figure 1.2 (b). During the solder reflow process, the solder alloy is homogenized, and the solder bump shape becomes spherical. In the mean time, intermetallic compounds are formed between the solder and the under-bump metallization. The wafer is subsequently diced into individual chips after solder reflow. The flip chip is aligned to the substrate, as shown in Figure 1.2 (c), and all connections are made simultaneously during a solder reflow, as shown in Figure 1.2 (d). Finally, a polymeric underfill is applied to reinforce the solder joints and relieve stress due to the coefficient of thermal expansion (CTE) mismatch between the silicon chip and the substrate, as shown in Figure 1.2 (e).

1.2 PB-FREE SOLDER MATERIALS

Pb-Sn alloys have been used as the soldering materials for flip chip technology since IBM developed the C4 process [1.7]. The original C4 solder bumps contained very high Pb composition, and the most effective chip connection was achieved for 95% Pb / 5% Sn solder on the chip side, and 90% Pb / 10% Sn on the substrate side [1.7].

However, a change from Pb-bearing to Pb-free soldering materials has been driven by the global demand for eco-friendly electronic products [1.11]. A fairly large number of Pb-free solders have been described. In a review, Abtew and Selvaduray [1.12] reported 69 Pb-free solder alloys. One of the leading candidates for Pb-free solder is a eutectic Sn-Ag. The eutectic composition is 96.5 wt % Sn-3.5 wt % Ag, and has a melting point of 221 °C. The eutectic Sn-Ag is the solder material used in the aging and electromigration experiments that are reviewed in Chapter 2. The results of these two experiments were used in the analytical study described in Chapter 4 and Chapter 5.

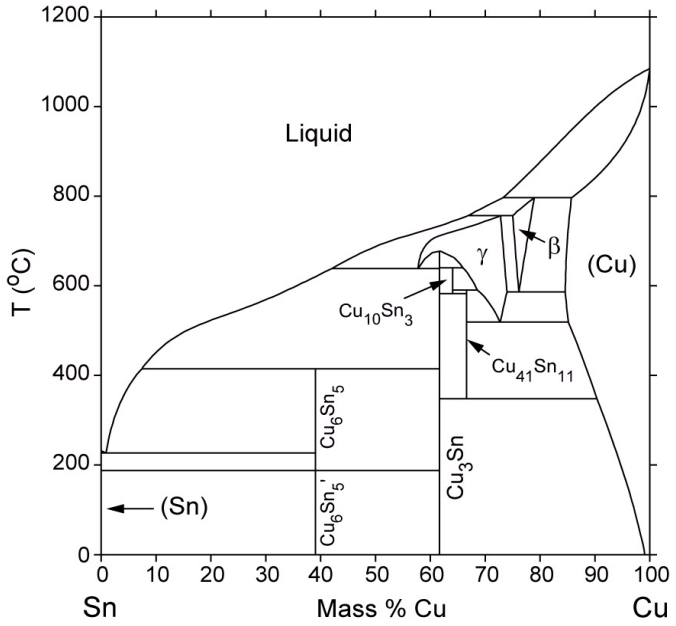
The reflow reaction of eutectic Sn-Ag solders on Cu under-bump metallization is expected to be very similar to that of pure Sn solders. The Ag-Cu phase diagram in Figure 1.4 shows no Ag-Cu intermetallic compound. Therefore, only Sn-based intermetallic compounds will form. The Cu-Sn phase diagram (Figure 1.5) shows that two intermetallic compounds, Cu_3Sn and Cu_6Sn_5, will form during reflow of Sn-based solders on Cu under-bump metallization.



(Source: Metallurgy Division of Material Science and Engineering Laboratory, National Institute of Standard and Technology (NIST) in Ref [1.11])[1]

Figure 1.4: Ag-Cu phase diagram

[1] Reused with permission from Metallurgy Division of Material Science and Engineering Laboratory, NIST.



(Source: Metallurgy Division of Material Science and Engineering Laboratory, NIST in Ref [1.11])[2]

Figure 1.5: Cu-Sn phase diagram

1.3 ELECTROMIGRATION

The term electromigration describes the transport of atoms in a metal subject to an applied electric field. It is an atomic diffusion process with a driving force, and therefore the drift velocity of the metal ions can be expressed by the Nernst-Einstein equation:

$$v_d = \mu F = \frac{D}{kT} F \tag{1.1}$$

[2] Reused with permission from Metallurgy Division of Material Science and Engineering Laboratory, NIST.

where μ is the ion mobility, D is the diffusivity, k is Boltzmann's constant, T is the absolute temperature in degree Kelvin and F is the electromigration driving force. The Nernst-Einstein equation is a general description of the drift of a species when it is subject to the influence of an external force. Studies of the electromigration driving force can be roughly classified into two parts, physical and phenomenological. The physical study aims to provide a fundamental understanding of the interactions of charges and moving atoms, when a metal is subjected to an electric field. The phenomenological study focuses on an investigation of the drift behaviors of the atoms and their correlation with the measurable effective electromigration driving force. In the phenomenological approach, the effective electromigration driving force is a mathematical expression of the correlation between the applied electric field and the observed drift phenomena. It does not employ a rigorous derivation of the physical origin of the electromigration driving force.

1.3.1 Electromigration in Bulk Metals

In most of the early work on electromigration, the driving force was considered to result from a reduction in the electrical potential energy when the metal atoms migrate in response to the electrical field as shown in Figure 1.6 [1.13]. Seith and Wever [1.14] were the first to conduct systematic studies on the electromigration driving force in metallic solids. Their work showed that the direction of mass transport depends on the type of prevailing charge carriers (electrons or holes) that are active in the metals of interest. In order to explain their result, they adopted the concept of an "electron wind" proposed by Skaupy [1.15]. This suggests that the momentum exchange of the atoms with moving charges contributes to the driving force for electromigration. Motions of this type are illustrated in Figure 1.7.

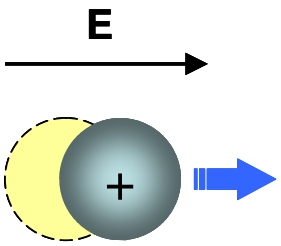


Figure 1.6: Movement of a metal ion under static electric field

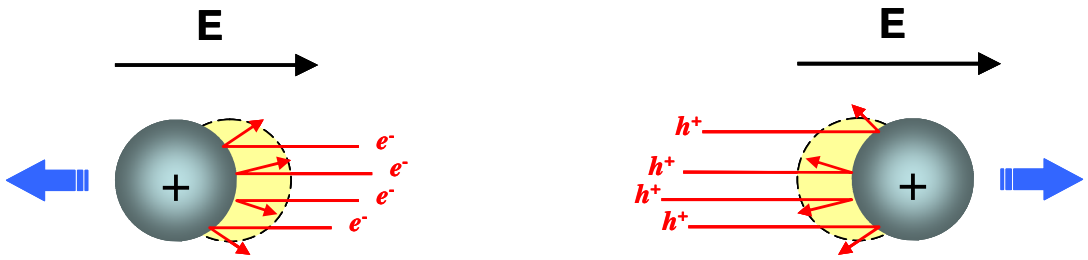


Figure 1.7: Movement of metal ions driven by the momentum exchange with the prevailing charge carriers: (a) negatively charged electrons are the prevailing charge carriers, and (b) positively charged electron holes are the prevailing charge carriers.

The formulation of the "electron wind" concept was approached independently by Fiks [1.17] and Huntington and Grove [1.18]. Semi-classical ballistic models were employed in their analysis to account for the electron wind effect. According to these models, the charge carriers flow in response to the static electric field and their momentum can be transferred to the static atoms on collision. The static atoms can be displaced from the original lattice sites due to the momentum transfer. The electron wind force can therefore be estimated by measuring the atomic drift. Bosvieux and Friedel [1.19] formulated the first quantum mechanical model of the electromigration driving force. However, it was indicated in a review that the wind force derived in their approach

becomes identical to that of the ballistic model if the quantum mechanical calculation is carried out to the first order [1.20].

The studies mentioned above represent the early research in the physics of the electromigration driving force. However, for applied research, a phenomenological description of the electromigration is more useful because it provides a direct correlation of the applied electric field and the measurable observation of the atomic drift. In a review, Huntington [1.20] approached the electromigration driving force within the framework of irreversible thermodynamics. Using his approach, the effective electromigration driving force can be expressed in terms of an effective charge Z^* based on the component interactions in the lattice.

$$\begin{aligned} F_{eff} &\equiv eZ^*E \\ &= e\left(Z^e + Z^w\right)E \end{aligned} \tag{1.2}$$

where e is the electronic charge and E is the electric field. Z^e is the valence of the ion in the lattice and Z^w is a virtual charge number that accounts for the electron wind force. The sum of the two, Z^*, known as the "effective charge number", provides a measure of the electromigration driving force.

By substituting Equation (1.2) into Equation (1.1), the drift velocity of the moving species can then be expressed as

$$v_d = \frac{D}{kT} eZ^*E \tag{1.3}$$

In the generalized electrostatic expression, the electric field can be described as the negative gradient of the electric potential

$$E = -\nabla \phi$$

where $\phi(x,y,z)$ is a scalar field representing the electric potential at a given point.

The atomic flux induced by electromigration can be expressed as the product of v_d, the drift velocity, and C_0, the atomic density of the moving species.

$$J = C_0 v_d = C_0 \frac{D}{kT} e Z^* E \tag{1.4}$$

It is apparent from Equation (1.4) that the effective charge number Z^* is the parameter describing the propensity of the ions to be displaced by the applied electric field. However, the diffusion behavior due to electromigration is related to both Z^*, the effective charge number, and D, the intrinsic diffusivity of the moving species of question. Ho and Kwok [1.21] provided a detailed review on the research activities dedicated to obtaining the effective charge numbers of various metals and alloys. This dissertation focuses on the study of a high-Sn Pb-free solder on Cu under-bump metallization. Cu is one of the noble metals and Sn is a quadrivalent metal. Table 1.1 shows the effective charge numbers derived for these two groups of metals. This table was originally compiled by H. B. Huntington in Ref [1.22].

Table 1.1: Effective charge numbers of selected metals (Source: Selected data from the original compilation by H. B. Huntington in Ref [1.22])

Metal	Z*	Temperature (°C)	Reference
Noble metals			
Gold	9.5 to 7.5	850-1000	[1.18]
	8.0		[1.23]
Silver	21±5	830-890	[1.20]
	8.3±1.8	795-900	[1.24]
Copper	2.0 to 5.0	800-900	[1.25]
	5.5±1.5	845-1030	[1.26]
Quadrivalent metals			
Lead	47	250	[1.20]
Tin	18	180-213	[1.27]

1.3.2 Electromigration in Fine Interconnect Lines

Electromigration was identified as the cause of the failure of aluminum interconnects in early integrated circuits [1.1]. This observation stimulated new and vigorous research activities, and the study in electromigration has since focused mostly on very practical problems related to damage formation in interconnects and its implication in the reliability of the integrated circuits.

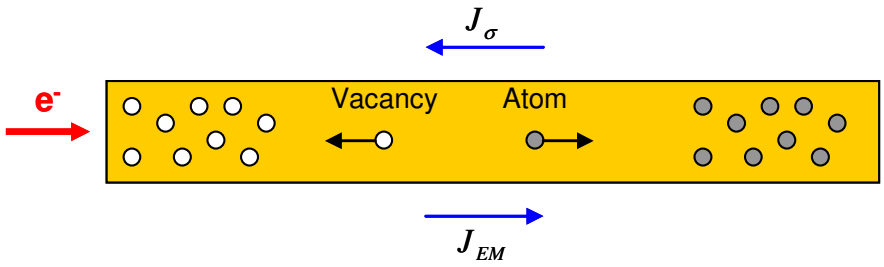
In a fine interconnect line, the electron flux distribution is uniform in the cross section of the line. The electric field can be expressed as the product of the current density and the resistivity of the metal. The atomic flux induced by the electromigration driving force, Equation (1.4), can, therefore, be rewritten as follows.

$$J = C_0 \frac{D}{kT} eZ^* \rho j \tag{1.5}$$

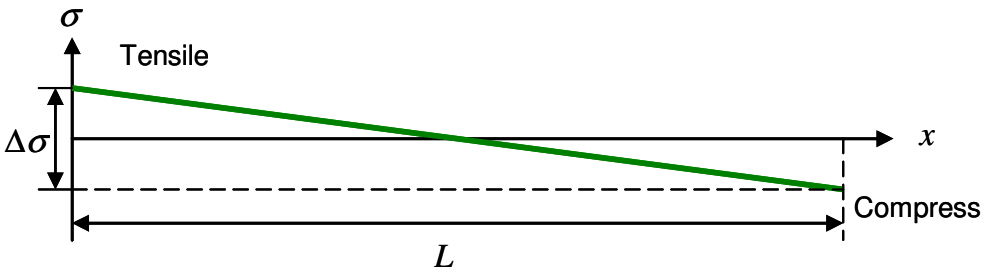
where ρ is the resistivity and j is the current density. Although the derivation of Equation (1.5) appears to be fairly straightforward, two characteristic phenomena play critical roles in the electromigration behavior observed in interconnect lines: stress-induced atomic backflow and fast diffusion paths.

1.3.2.1 Stress-Induced Backflow (Blech Effect)

While performing an electromigration experiment on aluminum thin film strips, Blech [1.28] discovered that the drift velocity was a function of the strip length and, more surprisingly, drift did not occur below a critical strip length. He rationalized that the atomic flux induced by the electromigration driving force was counteracted by a diffusional backflow relating to the strip length. It was suggested that the backflow is caused by the gradient of stress that builds up between the strip ends due to the electromigration-induced flux. The Blech effect is shown in Figure 1.8 for an aluminum line stressed by an applied current.



(a)



(b)

Figure 1.8: Stress induced backflow inside an aluminum wire: (a) mass transport, and (b) the stress state under electromigration

Figure 1.8 shows how electron flow enters the interconnect from the left and exits to the right. At the left end of the wire, tensile stress builds up due to net accumulation of vacancy. At the right end of the wire, compressive stress builds up due to net accumulation of atoms. The stress gradient can cause an additional flux opposing the electromigration induced flux.

The backflow resulting from the stress gradient can be expressed as:

$$J_\sigma = C_0 v_b = -C_0 \frac{D}{kT} \Omega \frac{\Delta\sigma}{\Delta x} \tag{1.6}$$

where v_b is the backflow drift velocity caused by stress gradients, Ω is the atomic volume, $\Delta\sigma$ is the difference between the stress at the compressive region and the stress at and tensile region, and $\Delta x \approx L$ is approximately the length of the interconnect line. The total atomic flux under electromigration is expressed as follows.

$$J = J_{EM} + J_\sigma = C_0 \frac{D}{kT} eZ^* \rho j - C_0 \frac{D}{kT} \frac{\Delta\sigma\Omega}{L} \tag{1.7}$$

In Equation (1.7), if the total flux becomes zero ($J = 0$), the diffusive flux induced by the electromigration driving force is completely counteracted by the backflow. Under this condition, the net mass transport vanishes. By letting $J = 0$ and rearranging Equation (1.7), one can show that the threshold condition for net zero mass transport to occur is the following.

$$(jL)_c = \Omega \frac{\Delta\sigma}{Z^* e \rho} \tag{1.8}$$

In Equation (1.8), Ω, Z^*, and ρ are properties of the metallization material. However, $(jL)_c$ can be maximized through the optimization of the dielectric materials and the design of the structure layout.

1.3.2.2 Damage Formation

The dominant electromigration failure mode is void formation which causes open-circuit failure. Under electromigration, void formation is typically controlled by diffusion flux divergence and fast diffusion paths. Flux divergence causes a net loss of mass in a local region, and only a small amount of material depletion is needed to cause failure. Fast diffusion paths provide pathways that allow mass transport to occur at a rate substantially faster than in the bulk material, and significantly reduce the interconnect lifetime. It is widely known that the dominant diffusion path for copper interconnects is at the interface between copper and the capping layer [1.29].

1.3.3 Electromigration in Flip Chip Solder Joints

Electromigration has only recently become widely accepted as a reliability concern for solder bumps. The accelerated lifetime experiments for interconnect technology are usually conducted at the current density level of 10^6 Amp/cm^2 [1.29]. However, studies have shown that electromigration-induced damage affect the lifetime of solder bumps at a current density two orders of magnitude lower, at the level of 10^4 Amp/cm^2 [1.2, 1.3]. This phenomenon results from the fact that different damage formation mechanisms are operative in solder bumps and in interconnect lines.

As described in previous section, the electromigration induced damage in interconnect wires is mainly attributed to diffusion flux divergence and fast diffusion paths. Self diffusion is almost negligible because the interconnect conductors are predominantly pure metal copper. The solder joint, however, is a much more complex material system because it involves multiple elements and phases. The solder material is usually tin or a tin-based alloy. The under-bump metallization is typically made of copper or nickel. Intermetallic compounds form between the solder and the under-bump metallization during reflow and continue to grow in aging conditions. When the solder is subjected to an electromigration driving force, electron flux flows across the multi-phase system. Both electromigration and concentration-driven interdiffusion are active. The diffusion behavior in the multi-phase multi-element alloy system is usually very complex because the diffusivities of the various species can be different. Under electromigration, vacancy transport plays a critical role in controlling the void formation and the lifetime of the solder joints.

Intermetallic compound growth and void formation occur in the Sn-based solders on Cu under-bump metallization. Compared to the conventional high Pb solders, these

behaviors can take place more rapidly and more extensively. This is because of the following reasons: First, Sn forms a number of Cu-Sn intermetallic compounds but Pb does not form compounds with Cu. Therefore, solders with a high Sn content provide an ample supply of Sn atoms for the compound formation. Second, Cu atoms diffuse very rapidly in the Sn lattice because the diffusion occurs in an interstitial process. When the solder joint is subjected to current stressing, fast diffusion of Cu can greatly enhance net mass loss at the cathode side (entrance of electron flux) and shorten the solder lifetime [1.2, 1.3, 1.16]. Therefore, the following phenomena are critical to the understanding of the damage formation in solder joints subject to electromigration, and were studied in this dissertation via an analytical model.

1. Concentration-driven diffusion
2. Intermetallic compound growth
3. Electromigration induced diffusion
4. Electromigration-enhanced vacancy transport

1.4 OBJECTIVE AND APPROACH

The objective of this work was to establish an analytical model and simulation for electromigration enhanced intermetallic compound growth and void formation in Pb-free solders through analytical modeling that takes into account interdiffusion and electromigration. The model derives from measurements reported by others that are explicitly referenced in the appropriate sections. The key contributions of this dissertation are as follows:

Intermetallic Compound Kinetics Modeling:

A finite difference model was established to study the electromigration-enhanced interdiffusion problem of a high-Sn Pb-free solder on Cu under-bump metallization. To the best knowledge of the author, this is the first modeling study that takes into account multiple intermetallic phases in the analysis of the electromigration-enhanced kinetics of solder-UBM alloying systems. The model formulation and generation are described in Chapter 3. The analysis conducted with this model is given in Chapter 5.

Derivation of Diffusion and Electromigration Parameters

Quantitative modeling requires knowledge of certain parameters to make meaningful predictions. In electromigration studies, these parameters include the diffusion coefficients and effective charge numbers for both diffusants, Cu and Sn atoms, in all four phases. However, these critical parameters have not been reported for the intermetallic compounds. Direct measurement of these parameters is difficult for the following reasons: a) These compounds are thin layers between Cu and Sn phases; b) they have characteristic morphologies and a tendency to grow. It is proposed in this dissertation that these parameters can be obtained by analyzing the compound growth kinetics. The simulated annealing method was used to deduce these parameters efficiently from the experimentally observed compound growths. This is described in Chapter 4.

Chapter 2: Solder Reactions

2.1 INTRODUCTION

This chapter first reviews the solder reflow reaction because the reflow process directly affects the initial compound thickness and the morphology of the solder bumps investigated in this study. This chapter also describes the thermal aging and electromigration experiments, the results of which are used to verify the intermetallic compound growth model. The experiments reviewed in this chapter were conducted by other authors, and are explicitly referenced.

2.2 REFLOW

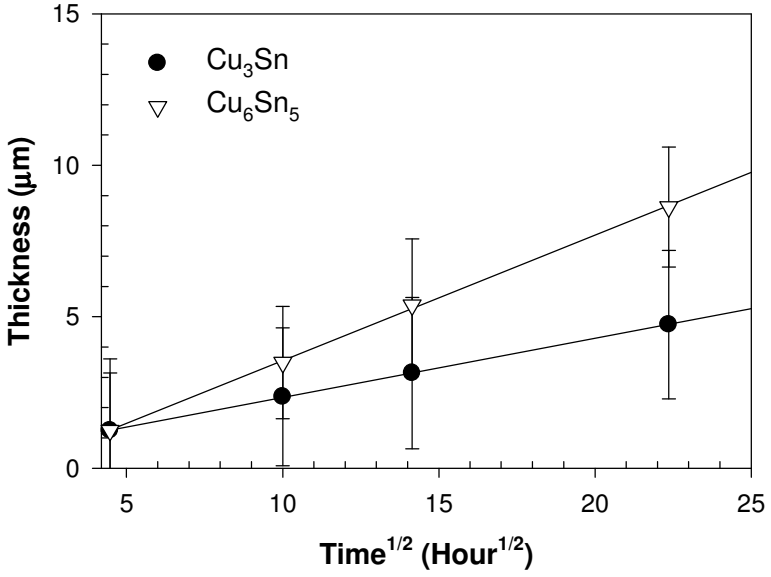
In flip chip technology, intermetallic bonding occurs between the solder material and the under-bump metallization during solder reflow. For Sn-based solders on Cu under-bump metallization, two intermetallic compounds, Cu_3Sn and Cu_6Sn_5, can form during solder reflow. Cu_3Sn is formed in a thin layer adjacent to the Cu under-bump metallization whereas the Cu_6Sn_5 phase has a characteristic scallop-like morphology and forms between Cu_3Sn and the Sn solder [2.1].

However, Cu_6Sn_5 does not always form in the scallop morphology. Tu [2.2] showed that the Cu_6Sn_5 phase forms in a layer morphology if the formation of the intermetallic phase is driven only by solid state interdiffusion between Sn and Cu. This observation showed that the formation of the scallop morphology by Cu_6Sn_5 occurs by a liquid/solid interfacial reaction between the molten solder and the intermetallic compound.

2.3 AGING EXPERIMENT [2.3]

For solid state aging of eutectic Sn Pb solder, Tu *et al*. [2.4] found that the Cu_6Sn_5 morphology gradually changed from the scallop type, as formed in reflow, to the layer type. They indicated that the solid state aging kinetics follows a parabolic law, suggesting a diffusion-controlled mechanism. Their results confirmed that the layered structure is the stable morphology for Cu_6Sn_5. The scallop type morphology observed in the solder joints is a product of the liquid/solid interfacial reaction during solder reflows.

The aging data reported by Siewert *et al*. [2.3] were used in this dissertation to verify the modeling of the intermetallic compound growth kinetics during thermal aging. In their experiment, the sample substrates were first plated with 45–50 μm of Cu. Sn–3.5Ag solder was deposited onto the Cu layer by melting the solder at 50 °C above the melting temperature. The samples were then thermally aged in an oven at 150 °C, which was purged with industrial-grade Ar gas to prevent oxidation during thermal aging. The thickness of the intermetallic growth was determined for each phase by examination of specimen cross section in a scanning electron microscope (SEM). Figure 2.1 shows the intermetallic compound growth in their thermal aging experiment. The trend lines were empirically fit and were not generated by the physical model. The error bars resulted from the uneven interfaces during intermetallic compound growth and the data points were the average of at least 20 measurements at different locations on the samples. The two intermetallic compounds Cu_3Sn and Cu_6Sn_5 could be distinctly identified after 100 hours of thermal aging.



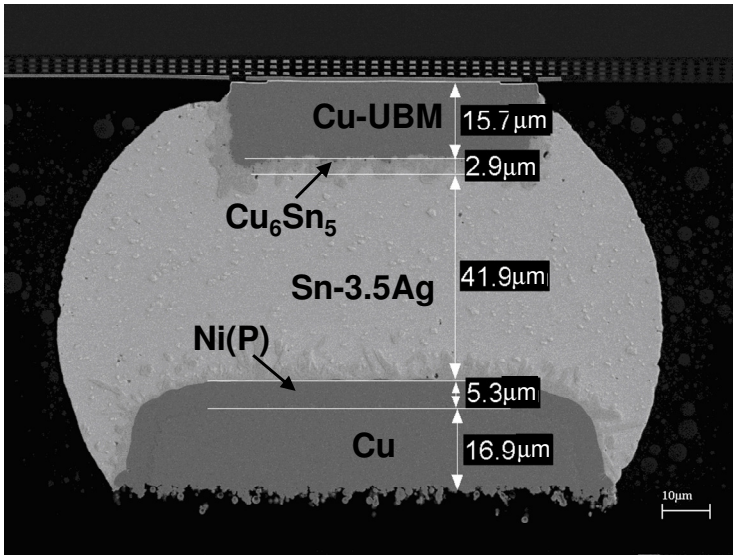
(Source: T. A. Siewert *et al.* in Ref [2.3])[3]

Figure 2.1: Intermetallic compound growth during thermal aging

2.4 ELECTROMIGRATION EXPERIMENT [2.5]

The electromigration data reported by Chae [2.5] were used to verify the modeling results of the intermetallic compound growth under electromigration. His experiment is described as follows. Sn-3.5Ag solder bumps with Cu under-bump metallization, as shown in Figure 2.2, were used. Note that the Cu under-bump metallization, the entrance of the applied electron flux, is at the top of the micrograph and the Cu top surface metallurgy, the exit of the applied electron flux, is at the bottom of the micrograph. In this figure, the Cu_6Sn_5 thickness was only roughly estimated, and the Cu_3Sn phase was reported to be a thin layer (~0.16 μm) between the Cu_6Sn_5 and the Cu under-bump metallization.

[3] Controbution of NIST; not subject to copyright in the U.S.



(Source: S.–H. Chae in Ref [2.5])[4]

Figure 2.2: Sn-3.5Ag solder joint with Cu under-bump metallization used for electromigration experiment (metrology added by the author)

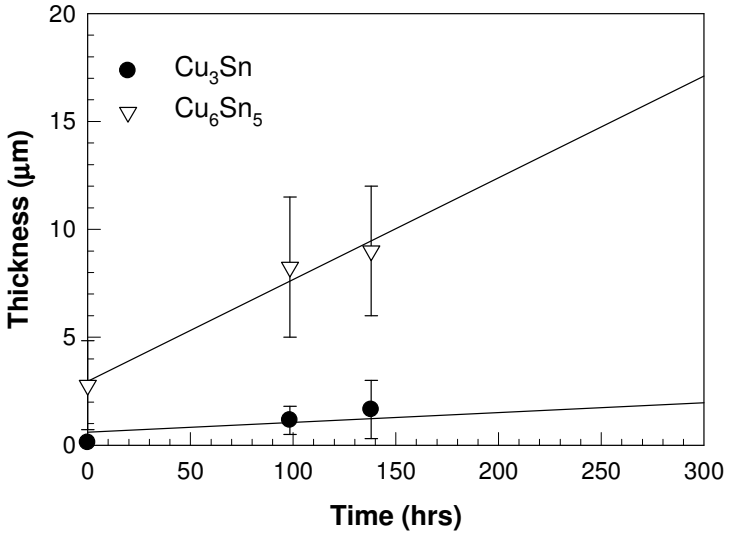
During the electromigration tests, the test structures were subjected to a high current stressing (4.12×10^4 and 5.16×10^4 Amp/cm^2) at an elevated temperature (~140 °C) for a prolonged period of time (>400 hr). Electron current flowed from the under-bump metallization to the top surface metallurgy. The current density was calculated by dividing the current by the area of the opening between the Cu interconnect and the Cu under-bump metallization. To reduce joule heating, which can raise the solder temperature, all specimens were attached to a Cu plate in the Si die side. This Cu plate was used to dissipate heat from the test structure. Thermocouples were attached between the Si dies and the Cu plate to provide a measurement of the temperature at the backside of the Si die. The oven temperature was adjusted so that the Si backside temperature of the samples was kept steady at 140 °C. In order to obtain an estimate of the solder

[4] With kind permission from S.-H. Chae, Master Report, the University of Texas at Austin, August 2006.

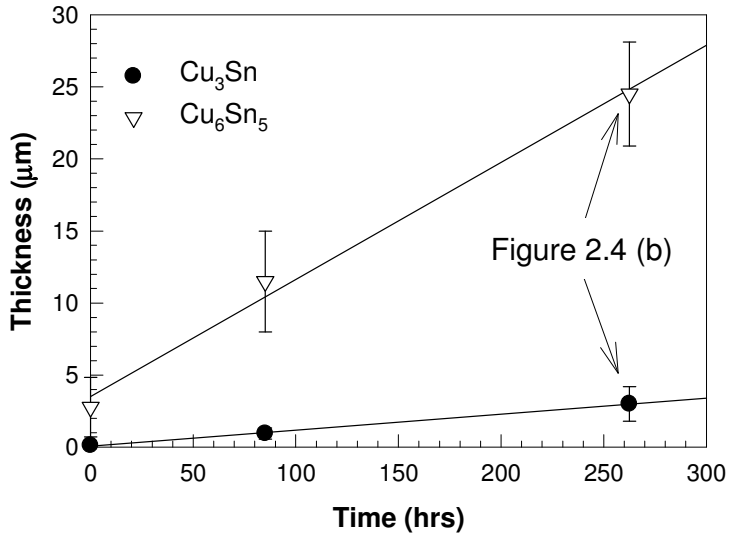
temperature, Joule heating must be accounted for. The detailed methodology of Joule heating analysis is described in Appendix A. The result of the Joule heating analysis indicated that the solder temperature was 10 to 15 °C above the measured Si backside temperature, that is, 150 to 155 °C. In this study, the model used 150 °C as the solder temperature.

Cross-sectional micrographs were acquired using scanning electron microscopy (SEM) to investigate the intermetallic growth and void formation. Each phase was identified by energy-dispersive X-Ray spectroscopy analysis (EDX) performed in the SEM. Due to the non-planar nature of the Cu_6Sn_5 layer, the nominal thickness was estimated by dividing the cross-sectional area of the intermetallic compound by the initial width of the corresponding under-bump metallization. Figure 2.3 (a) and (b) show the intermetallic compound growth under two current stressing conditions: 4.12×10^4 Amp/cm^2 and 5.16×10^4 Amp/cm^2. The trend lines in the plots were empirically fit and were not generated by the physical model.

Electromigration induced damage has been observed to control the lifetime of solder joints in accelerated current stress tests [2.5, 2.6]. Brandenburg and Yeh [2.7] studied the effect of electromigration on the lifetime of eutectic SnPb solder joints and reported the failure mechanism to be void formation at the cathode side (entrance of electron flux) of the solder joint. They proposed a void formation mechanism induced by local vacancy super-saturation, but vacancy kinetics was not investigated in their study.



(a)



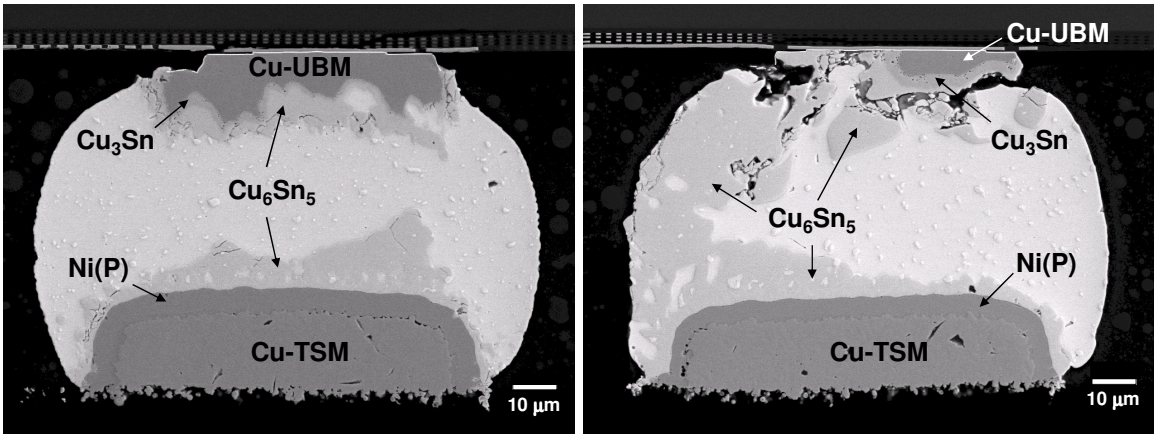
(b)

(Source: S.–H. Chae in Ref [2.5])[5]

Figure 2.3: Intermetallic compound growth under current stressing: (a) 4.12×10^4 Amp/cm^2 and (b) 5.16×10^4 Amp/cm^2; the trend lines were empirically fit

[5] With kind permission from S.-H. Chae, Master Report, the University of Texas at Austin, August 2006.

Figure 2.4 shows damage evolution in the solder joint that was observed in Chae's electromigration experiment [2.5]. When electromigration caused the Cu under-bump metallization to dissolve into the Pb-free solder, as shown in Figure 2.4 (a), the intermetallic compounds grew in the layered-like fashion. Therefore, the one dimensional model is assumed to be valid for the evaluation of the intermetallic compound growth. Toward the end of the solder lifetime, as shown in Figure 2.4 (b), the morphology of the intermetallic compounds deviated from layers parallel to the original under-bump metallization. This condition corresponds to the data obtained at 263rd hour in Figure 2.3 (b) and these data points were only used as a reference in the model. The ultimate open-circuit failure of the solder joints occurred when the majority of the Cu under-bump metallization was consumed and voids formed extensively.



(a) (b)

(Source: S.–H, Chae in Ref [2.5])[6]

Figure 2.4: Electromigration damage evolution

[6] With kind permission from S.-H. Chae, Master Report, the University of Texas at Austin, August 2006.

Chapter 3: Electromigration Enhanced Intermetallic Kinetics

3.1 INTRODUCTION

A common failure mode for flip chip packages is an electrical open circuit generated by void formation induced by intermetallic compound (IMC) growth at the interface between the solder and under-bump metallization (UBM). Failures of this type have been reported after prolonged current stressing at an elevated temperature and have been shown to result from electromigration [3.1, 3.2]. Under electromigration, intermetallic compound growth can be significantly enhanced and accompanied by void formation, which plays an important role in controlling the electromigration lifetime of the solder joints in flip-chip packages [3.3, 3.4]. Gan and Tu [3.5] reported distinct characteristics for intermetallic compound growth at the anode and at the cathode, and they formulated a kinetic model to account for this current polarity effect. In their model, the two intermetallic phases, Cu_3Sn and Cu_6Sn_5, were not distinguished, but were instead treated as a single phase for simplicity. Following this study, Orchard and Greer [3.6] approached this problem through a theoretical analysis, taking into account the effect of interfacial reaction barriers; however, their analysis still treated only a single intermetallic phase.

Gurov and Gusak [3.7] were the first to consider the formation of two intermetallic compounds under an electric field. They found that growth kinetics can follow distinct growth modes depending on the balance of the interdiffusion and electromigration fluxes in the individual compound layers. Nevertheless, due to a lack of pertinent parameters, their study was limited to a generalized discussion of the growth modes and no quantitative analysis was provided.

3.2 ELECTROMIGRATION IN PB-FREE SOLDERS ON CU UBM

3.2.1 Interdiffusion in Substitutional Alloys

A Cu-Sn diffusion couple is considered, in which two intermetallic phases, Cu_3Sn and Cu_6Sn_5, form between pure Cu and pure Sn phases, as shown in Figure 3.1. Within each phase, interdiffusion of Cu and Sn atoms occurs simultaneously. In addition, the electron current from the under-bump metallization (UBM) toward the top surface metallurgy (TSM) exerts a directional driving force causing atoms to diffuse in this direction. Darken's [3.8] equation for interdiffusion can be modified to apply to this particular case, so that atomic fluxes induced by the concentration gradient and by the external electric field can both be taken into account.

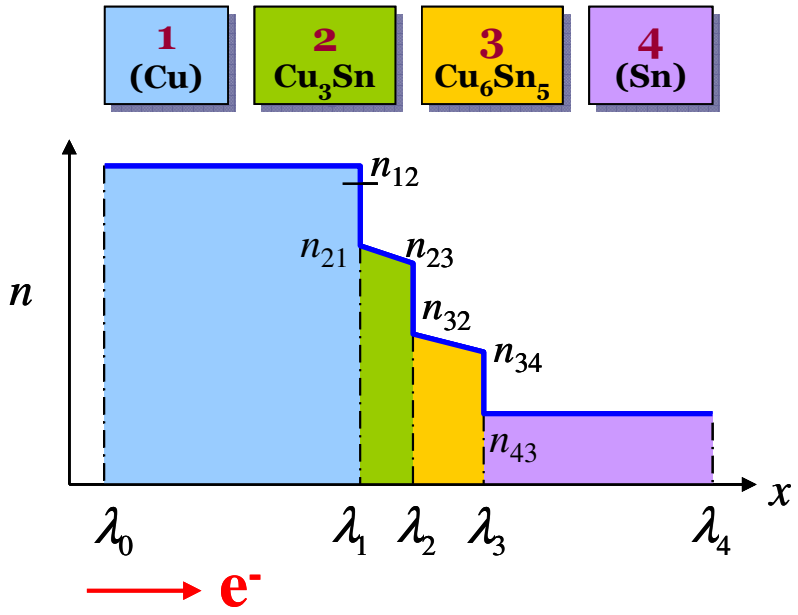


Figure 3.1: Composition profile in the layered structure of a Cu-Sn diffusion couple (*n* is the composition in atomic fraction of Cu).

The two intermetallic phases have narrow composition ranges as indicated by the Cu-Sn phase diagram shown in Figure 1.5. Table 3.1 lists the composition limits of each phase at 150 °C. The derivation of these values is described in Appendix B.

Table 3.1: Composition limits (in atomic fraction of Cu) of the terminal and intermetallic phases in a Cu-Sn diffusion couple at 150 °C

n_{12}	n_{21}	n_{23}	n_{32}	n_{34}	n_{43}
0.995	0.755	0.749	0.552	0.545	0.001

Note: See Appendix B

The concentrations are described as follows.

$$C_{Cu}=C_0 n_{Cu}$$

$$C_{Sn}=C_0 n_{Sn}$$

where C_0 is the atomic density. The atomic densities are assumed to be constant within each phase and their values are given in Table 3.2. The concentrations of the Cu and Sn atoms are C_{Cu} and C_{Sn}. The atomic fractions of the Cu and Sn atoms are n_{Cu} and n_{Sn}. For the remaining formulation, the composition is represented in atomic fraction of Cu unless denoted otherwise, and the subscript $_{Cu}$ is omitted. It is also assumed that the vacancy concentration is low and therefore $n_{Cu}+n_{Sn}=1$, that is, $C_{Cu}+C_{Sn}=C_0$.

Table 3.2: Atomic densities of the phases in the Cu-Sn diffusion couple

Phase	Cu	Cu_3Sn	Cu_6Sn_5	Sn
C_0 (mol/m^3)	0.141	0.115	0.094	0.062

Note: See Appendix F

During self-diffusion in a crystalline metal, all atoms are presumably identical. Therefore, the probability is equivalent for any given atom to be adjacent to a vacancy and have sufficient energy to make a jump into it. In substitutional alloys, however, the rates at which different component elements can move into a vacant site are not equal. Thus each atomic species must be given its own *intrinsic* diffusion coefficient when calculating its diffusive flux.

The atomic fluxes due to chemical diffusion are expressed as

$$J_{Cu,i}^{Chem} = -D_{Cu,i}\frac{\partial C_i}{\partial x}$$

$$J_{Sn,i}^{Chem} = -D_{Sn,i}\frac{\partial C_{Sn,i}}{\partial x} = D_{Sn,i}\frac{\partial C_i}{\partial x} \qquad (3.1)$$

In these expressions, J is the diffusion flux, D is the diffusion coefficient, C is the concentration, x is the thickness and i is the index for the phases (pure Cu, Cu_3Sn, Cu_6Sn_5, or pure Sn). Therefore, Equations (3.1) are in fact eight independent partial differential equations.

The current-induced atomic fluxes are expressed as

$$J_{Cu,i}^{EM} = C_{Cu,i} \frac{D_{Cu,i}}{kT} Z_{Cu,i}^{*} e\rho_i j = C_i D_{Cu,i} \phi_{Cu,i} j$$

$$J_{Sn,i}^{EM} = C_{Sn,i} \frac{D_{Sn,i}}{kT} Z_{Sn,i}^{*} e\rho_i j = (C_{0,i} - C_i) D_{Sn,i} \phi_{Sn,i} j \tag{3.2}$$

where k is the Boltzmann constant, T is the absolute temperature in Kelvin, Z^* is the effective charge number, e is the electron charge, ρ is the resistivity, and ϕ is the electromigration factor described in Equation (3.3).

$$\phi = \frac{Z^*}{kT} e\rho \tag{3.3}$$

As a result, a diffusion flux is the composition of the fluxes induced by chemical diffusion and electromigration.

$$J_{Cu,i} = J_{Cu,i}^{Chem} + J_{Cu,i}^{EM}$$

$$J_{Sn,i} = J_{Sn,i}^{Chem} + J_{Sn,i}^{EM} \tag{3.4}$$

These fluxes are shown schematically in Figure 3.2. The chemical diffusion fluxes of the Cu and Sn atoms move in opposite directions because the Cu-rich source is the left phase and the Sn-rich source is the right phase. However, the electromigration induced fluxes move in the same direction as the electron flux. Clearly, the inequality holds true unless the fluxes moving in opposing directions exactly cancel out one another.

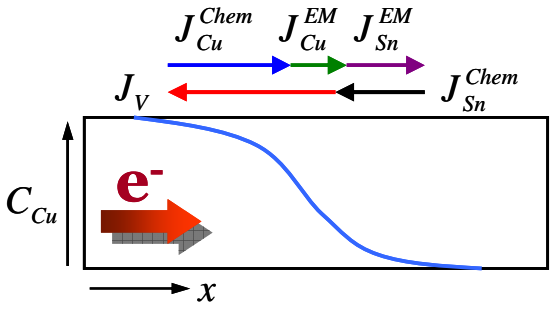


Figure 3.2: Concentration profile and diffusion fluxes during interdiffusion of the Cu-Sn binary alloy, which is adjacent to a Cu-rich phase to the left and a Sn-rich phase to the right.

$$J_{Cu,i} \neq -J_{Sn,i} \tag{3.5}$$

In substitutional alloys, atoms diffuse by jumping into an adjacent vacant site in the lattice. Conversely, the vacancy can be viewed as a diffusing entity that can jump into a site occupied by an atom. The diffusion fluxes can be balanced by introducing an additional vacancy flux.

$$J_{Cu,i} + J_{Sn,i} + J_{V,i} = 0 \tag{3.6}$$

By substituting Equations (3.4) into Equations (3.6), the vacancy flux can be expressed as

$$\begin{aligned} J_{V,i} &= -J_{Cu,i} - J_{Sn,i} \\ &= D_{Cu,i}\frac{\partial C_i}{\partial x} - D_{Sn,i}\frac{\partial C_i}{\partial x} - C_i D_{Cu,i}\phi_{Cu,i} j - (C_{0,i} - C_i) D_{Sn,i}\phi_{Sn,i} j \\ &= (D_{Cu,i} - D_{Sn,i})\frac{\partial C_i}{\partial x} - j\left[C_i D_{Cu,i}\phi_{Cu,i} + (C_{0,i} - C_i) D_{Sn,i}\phi_{Sn,i}\right] \end{aligned} \tag{3.7}$$

For substitutional alloys in which atoms migrate in a vacancy process, it is well established that the net flux of vacancies gives rise to the movement of the lattice [3.9]. This occurs mainly by two mechanisms. Vacancies can be absorbed at a jog on an edge dislocation, which will eventually lead to elimination of atomic planes. Vacancies can also be created at the jogged edge dislocation and the result can lead to insertion of new atomic planes. The velocity at which the atomic planes move is controlled by the vacancy flux, as described in the following equation:

$$u_i = \frac{J_{V,i}}{C_0} = \left(D_{Cu,i} - D_{Sn,i}\right)\frac{\partial n_i}{\partial x} - j\left[n_i D_{Cu,i}\phi_{Cu,i} + \left(1-n_i\right)D_{Sn,i}\phi_{Sn,i}\right] \tag{3.8}$$

The fluxes in Equations (3.1) through (3.4) are derived from the local driving forces so they are in fact based on a moving lattice. In order to derive the true fluxes in a fixed frame of reference relative to the specimen, a virtual flux $u_i C_i$ is added based on the velocity of the moving lattice, as expressed in Equation (3.9)

$$\begin{aligned}
J'_{Cu,i} &= J^{Chem}_{Cu,i} + J^{EM}_{Cu,i} + u_i C_i \\
&= -D_{Cu,i}\frac{\partial C_i}{\partial x} + C_i D_{Cu,i}\phi_{Cu,i}\, j + u_i C_i \\
&= -D_{Cu,i}\frac{\partial C_i}{\partial x} + n_i\left(D_{Cu,i} - D_{Sn,i}\right)\frac{\partial C_i}{\partial x} - C_i\, j\left[-D_{Cu,i}\phi_{Cu,i} + n_i D_{Cu,i}\phi_{Cu,i} + \left(1-n_i\right)D_{Sn,i}\phi_{Sn,i}\right] \\
&= -\left(n_{Sn,i}D_{Cu,i} + n_{Cu,i}D_{Sn,i}\right)\frac{\partial C_i}{\partial x} - C_i\, j\left(1-n_i\right)\left(D_{Sn,i}\phi_{Sn,i} - D_{Cu,i}\phi_{Cu,i}\right) \\
&= -\tilde{D}_i\frac{\partial C_i}{\partial x} - \frac{\tilde{\phi}_i\, j}{C_{0,i}}C_i\left(C_{0,i} - C_i\right)
\end{aligned} \tag{3.9}$$

where

$$\tilde{D}_i = n_{Sn,i} D_{Cu,i} + n_{Cu,i} D_{Sn,i} \tag{3.10}$$

$$\tilde{\phi}_i = D_{Sn,i} \phi_{Sn,i} - D_{Cu,i} \phi_{Cu,i} \tag{3.11}$$

Equation (3.10) describes an interdiffusion coefficient, $\tilde{D}_i$, which depends on both D_{Cu} and D_{Sn} of the phase in question. This was first proposed by Darken [3.8] when he formulated an expression describing the interdiffusion of substitutional alloys. This term remains the same after the electromigration effect is introduced to the formulation. Equation (3.11) describes a new term, $\tilde{\phi}_i$, the *effective interdiffusion electromigration coefficient*. It depends on temperature, resistivity, the diffusion coefficient and the effective charge number of the component elements.

One can also derive the true flux of Sn atoms similarly to Equation (3.9):

$$\begin{aligned} J'_{Sn,i} &= -\tilde{D}_i \frac{\partial C_{Sn,i}}{\partial x} + \frac{\tilde{\phi}_i j}{C_{0,i}} C_i \left(C_{0,i} - C_i \right) \\ &= -J'_{Cu,i} \end{aligned} \tag{3.12}$$

Fick's second law of diffusion applied to a substitutional alloy subject to current stressing now becomes:

$$\frac{\partial C_i}{\partial t} = -\frac{\partial J'_{Cu,i}}{\partial x}$$

or

$$\frac{\partial C_i}{\partial t}=\frac{\partial}{\partial x}\left[\tilde{D}_i\frac{\partial C_i}{\partial x}+\frac{\tilde{\phi}_i j}{C_{0,i}}C_i\left(C_{0,i}-C_i\right)\right] \tag{3.13}$$

Gurov and Gusak [3.7] first proposed this type of formulation in 1981 in a generalized discussion of interdiffusion in an external electric field. A very similar formulation is derived in the present study of Cu-Sn interdiffusion subject to current stressing.

3.2.2 Intermetallic Phase Growth

The previous section formulated expressions for the diffusion that takes place in each phase of the Cu-Sn diffusion couple. The analysis is based on phase kinetics driven by the concentration-induced and the electromigration-induced fluxes. A schematic of the layered structure of a Cu-Sn diffusion couple is shown in Figure 3.1. In order to derive the rate at which each phase grows or shrinks, one must consider mass transport across the interfaces.

Figure 3.3 describes the concentrations of two adjacent phases near their associated interface. In this diagram, α and β denote the two adjacent phases of interest. The concentration profile is a function of time t and spatial coordinate x, and it is controlled by the diffusion behavior in each phase. Therefore, it can be obtained using Equation (3.13). The concentrations at the interface, $C_{\alpha\beta}$ and $C_{\beta\alpha}$, are restricted by the solute solubility according to the pertinent phase diagram. As the interface moves to the left by a distance dx, for example, the number of Cu atoms dissolving from α into β can be expressed as $(C_{\alpha\beta}-C_{\beta\alpha})dx$. Conservation of Cu atoms dictates that the atomic flux of

Cu migrating across the interface must be balanced by the Cu flux in the two adjacent phases α and β in the vicinity of the interface.

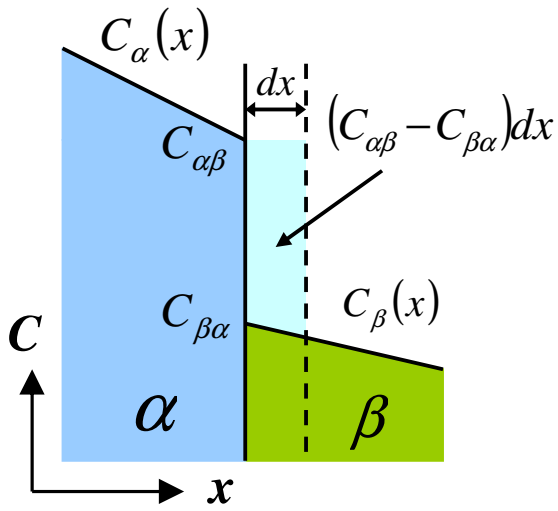


Figure 3.3: Concentration profile near an interface

$$(C_{\alpha\beta}-C_{\beta\alpha})dx=(J'_\alpha-J'_\beta)dt \tag{3.14}$$

Applying Equation (3.9) to both the α and β phases across the interface, the fluxes can be described as:

$$J'_\alpha=-\tilde{D}_\alpha\frac{\partial C_\alpha}{\partial x}-\frac{\tilde{\phi}_\alpha j}{C_{0,\alpha}}C_{\alpha\beta}(C_{0,\alpha}-C_{\alpha\beta})$$

$$J'_\beta=-\tilde{D}_\beta\frac{\partial C_\beta}{\partial x}-\frac{\tilde{\phi}_\beta j}{C_{0,\beta}}C_{\beta\alpha}(C_{0,\beta}-C_{\beta\alpha}) \tag{3.15}$$

The velocity of the interfacial movement can subsequently be derived using Equations (3.14) and (3.15).

$$
\begin{aligned}
v &= \frac{dx}{dt} = \frac{J'_{\alpha} - J'_{\beta}}{C_{\alpha\beta} - C_{\beta\alpha}} \\
&= \frac{1}{C_{\alpha\beta} - C_{\beta\alpha}} \left\{ \left(\tilde{D}_{\beta} \frac{\partial C_{\beta}}{\partial x} - \tilde{D}_{\alpha} \frac{\partial C_{\alpha}}{\partial x} \right) + j \left[\frac{C_{\beta\alpha} \left(C_{0,\beta} - C_{\beta\alpha} \right)}{C_{0,\beta}} \tilde{\phi}_{\beta} - \frac{C_{\alpha\beta} \left(C_{0,\alpha} - C_{\alpha\beta} \right)}{C_{0,\alpha}} \tilde{\phi}_{\alpha} \right] \right\} \\
&= v_{Chem} + v_{EM}
\end{aligned}
\tag{3.16}
$$

Each compound phase grows or shrinks in response to the movements of its interface boundaries. The velocity of the migrating interface, as described in Equation (3.16), is based solely on the conservation of Cu atoms across the interface. However, the rule of conservation for Sn atoms can also be applied using Equation (3.12). The resulting interfacial velocity, after rearranging the terms, is then identical to Equation (3.16). This is because Equation (3.6) dictates the correlation between the fluxes of the diffusing species: Cu atoms, Sn atoms, and vacancies. This check is critical, because the mass conservation rule must apply to both Cu and Sn atoms.

Finally, it is important to note that the formulation described in this chapter assumes that the phases of interest behave as substitutional alloys. That is, it is assumed that the solvent and solute atoms can occupy the same sites in the lattice without any preference. However, in the Cu-Sn interdiffusion system, the phases do not necessarily behave as substitutional alloys. In the pure Sn phase, Cu diffuses in an interstitial fashion in the Sn lattice [3.10]. The intermetallic compounds, Cu_3Sn and Cu_6Sn_5, are ordered alloys in which the lattice sites have strong preference for Cu or Sn atoms [3.11-3.13]. These properties have important consequences relative to the results of the analysis and will be discussed further in Chapter 4.

3.2.3 Vacancy Transport

Vacancy transport plays a critical role in void formation under electromigration. A net vacancy flux arises due to the unequal diffusivities of the species and the additional directed driving force of electromigration. Vacancies can be absorbed by internal boundaries or free surfaces, and therefore contribute to the driving force of void formation. The rate of increase or decrease in vacancy concentration, *R(x)*, is described by Equation (3.17).

$$R(x) = -\frac{\partial J_V}{\partial x} \tag{3.17}$$

Combining Equations (3.7) and (3.17), the rate of local vacancy concentration increase becomes

$$R(x) = \frac{\partial C_V}{\partial x} = -(D_{Cu} - D_{Sn})\frac{\partial^2 C}{\partial x^2} - \tilde{\phi} j \frac{\partial C}{\partial x} \tag{3.18}$$

At location $x = a$, if $R(a) > 0$, the vacancy flux that flows into the infinitesimal region is greater than the vacancy flux that flows out of the region. In order to maintain the equilibrium vacancy concentration, vacancies in this region have a tendency to be annihilated at dislocations, defects, or internal boundaries. If $R(a) < 0$, there is a tendency for vacancies to be created at this region. Figure 3.4 shows the vacancy flux in an interdiffusion system. In this study, the vacancy flux, J_V, and vacancy concentration increase rate, *R(x)*, are both calculated. The results and discussion are presented in Chapter 5.

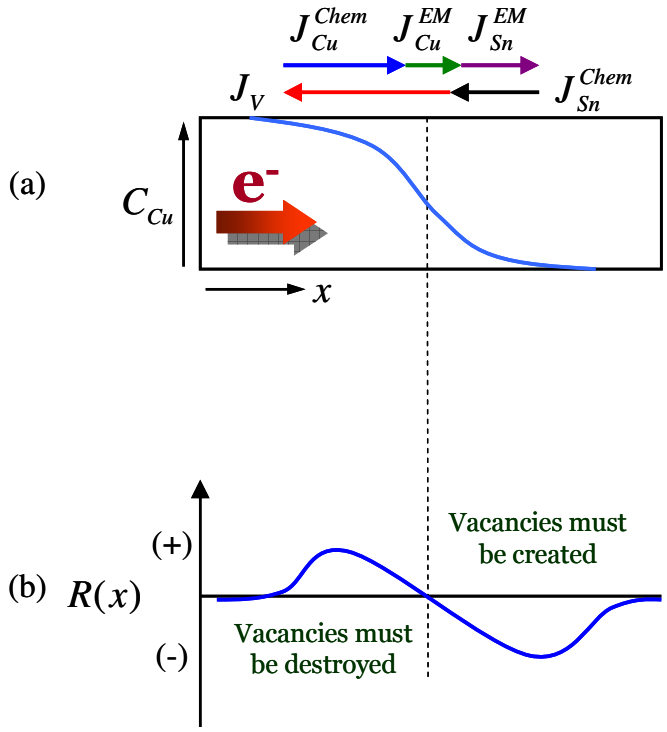


Figure 3.4: Interdiffusion and vacancy transport: (a) interdiffusion in a diffusion couple with fluxes due to various driving forces, and (b) the rate at which vacancy concentration can increase or decrease in a case where the vacancies are not created or destroyed at the vacancy sources or sinks.

3.3 FINITE DIFFERENCE MODEL

3.3.1 Mathematical Formulations

The object of this study is to model both the intermetallic compound growth and its associated vacancy transport when the Cu-Sn diffusion couple is subjected to both intrinsic interdiffusion and current stressing. Therefore, at least three sets of equations are required to solve this diffusion problem. First, an interdiffusion equation, Equation (3.13), is needed for each phase in the diffusion couple. Second, compound growth equations, such as Equation (3.16), describe the interfacial migration. Finally, the

vacancy fluxes are obtained using Equation (3.7) and vacancy increase rates are obtained using Equation (3.18) over the intermetallic phases.

These three sets of equations are highly correlated with one another. The concentration gradients at the vicinity of the interfaces are controlled by the interdiffusion equations and play an important role in controlling the rate at which the interfaces move. Both interdiffusion and interfacial migration play a role in controlling the concentration profile within the phase. The vacancy flux arises from both electromigration and Cu-Sn interdiffusion. Therefore, these equations must be addressed simultaneously. These equations are expressed in explicit form as follows, so that the constants and the independent variables are separated. The initial and boundary conditions are also given. The important parameters, such as diffusivity and electromigration parameters, are contained in lumped constants to facilitate program coding.

3.3.1.1 Current-Enhanced Interdiffusion

Equation

$$\frac{\partial}{\partial t}w_p(x,t)=\overline{A}\,w_p\frac{\partial^2}{\partial x^2}w_p+\overline{B}\frac{\partial^2}{\partial x^2}w_p+\overline{C}\left(\frac{\partial}{\partial x}w_p\right)^2+\overline{D}\,w_p\frac{\partial}{\partial x}w_p+\overline{E}\frac{\partial}{\partial x}w_p$$

for $\lambda_p \le x \le \lambda_{p+1}$ and $t \ge 0$

(3.19)

Initial Condition

$$w_p(x,0)=f(x)=C_{p,p-1}+\left(\frac{C_{p,p+1}-C_{p,p-1}}{\lambda_p^0-\lambda_{p-1}^0}\right)x \tag{3.20}$$

Boundary Conditions

Left: $$w_p(0,t)=C_{p,p-1} \tag{3.21}$$

Right: $$w_p(\lambda_p-\lambda_{p-1},t)=C_{p,p+1} \tag{3.22}$$

Constants

$$\overline{A}=\overline{C}=\frac{D_{Sn,p}-D_{Cu,p}}{C_{0,p}}$$

$$\overline{B}=D_{Cu,p}$$

$$\overline{D}=-\frac{2\tilde{\phi}_p j}{C_{0,p}}$$

$$\overline{E}=\tilde{\phi}_p j$$

The concentration function is $w_p(x,t)$, and the subscripts (p=1,2,3,4) indicate the phase. The interface concentration is C_{pq} and λ_p is the interface location, and the numbering of the phases is based on Figure 3.1. The diffusivity is D, $\tilde{\phi}$ is the interdiffusion electromigration factor indicated in Equation (3.11), and j is the current density.

Current-enhanced interdiffusion is time dependent and is described by a second-order nonlinear, partial differential equation. The nonlinear terms arise from the electromigration effect, as well as the unequal diffusivities of Cu and Sn atoms. The greatest challenge in determining the solution arises from the fact that the spatial domain

of this equation varies with time. As the intermetallic compound grows or shrinks, the spatial domain on which the interdiffusion takes place also expands or contracts.

A linear concentration profile is chosen as the initial condition for the two intermediate phases, because it provides a closed-form solution for steady-state diffusion, and is the most plausible "guess" for the initial concentration profile. The boundary conditions are given as the solubility limits based on the phase diagram.

The boundary phases are treated differently. Cu under-bump metallization is treated as a dissolving phase and Sn solder is treated as a phase saturated with Cu atoms. Explanation of the treatment of the boundary phases is given in Appendix D.

3.3.1.2 Interfacial Migration

Equation

$$\frac{d}{dt}\lambda_p(t) = \bar{a}\frac{\partial}{\partial x}\left[w_p\left(\lambda_p^-, t\right)\right] + \bar{b}\frac{\partial}{\partial x}\left[w_{p+1}\left(\lambda_p^+, t\right)\right] + \bar{c} \tag{3.23}$$

for $t \geq 0$

Initial Conditions

The initial conditions are based on the initial thickness of the intermetallic compounds as reported in Sections 2.3 and 2.4.

Constants

$$\bar{a} = -\frac{\left(C_{0,p} - C_{p,p+1}\right)D_{Cu,p} + C_{p,p+1}D_{Sn,p}}{C_{0,p}\left(C_{p,p+1} - C_{p+1,p}\right)}$$

$$\bar{b} = \frac{\left(C_{0,p+1} - C_{p+1,p}\right)D_{Cu,p+1} + C_{p+1,p}D_{Sn,p+1}}{C_{0,p+1}\left(C_{p,p+1} - C_{p+1,p}\right)}$$

$$\bar{c} = j\left[\frac{C_{p+1,p}\left(C_{0,p+1} - C_{p+1,p}\right)\tilde{\phi}_{p+1}}{\left(C_{p,p+1} - C_{p+1,p}\right)C_{0,p+1}} - \frac{C_{p,p+1}\left(C_{0,p} - C_{p,p+1}\right)\tilde{\phi}_{p}}{\left(C_{p,p+1} - C_{p+1,p}\right)C_{0,p}}\right]$$

The interfacial migration equation is a first-order time-domain differential equation. Therefore, only an initial condition is required; there are no boundary conditions necessary. The initial condition is the phase thickness as reported in Sections 2.3 and 2.4. This equation was coupled with the interdiffusion equation by determining the derivative of the concentration at each side of the interface.

3.3.1.3 Vacancy Transport

Equation

$$J_V(x,t) = \bar{\alpha}\frac{\partial w_p}{\partial x} + \bar{\beta} w_p + \bar{\gamma}$$

$$R(x,t) = -\left(\bar{\alpha}\frac{\partial^2 w_p}{\partial x^2} + \bar{\beta}\frac{\partial w_p}{\partial x}\right) \qquad (3.24)$$

for $\lambda_p \le x \le \lambda_{p+1}$ and $t \ge 0$

Constants

$$\bar{\alpha} = D_{Cu,p} - D_{Sn,p}$$

$$\bar{\beta} = \tilde{\phi}_p j$$

$$\gamma = -C_{0,p} D_{Sn,p} \phi_{Sn,p} j$$

3.3.2 Simulation Algorithm

Figure 3.5 shows the flowchart of the finite difference model that electromigration enhanced interdiffusion and intermetallic compound growth. Further detail are given as follows.

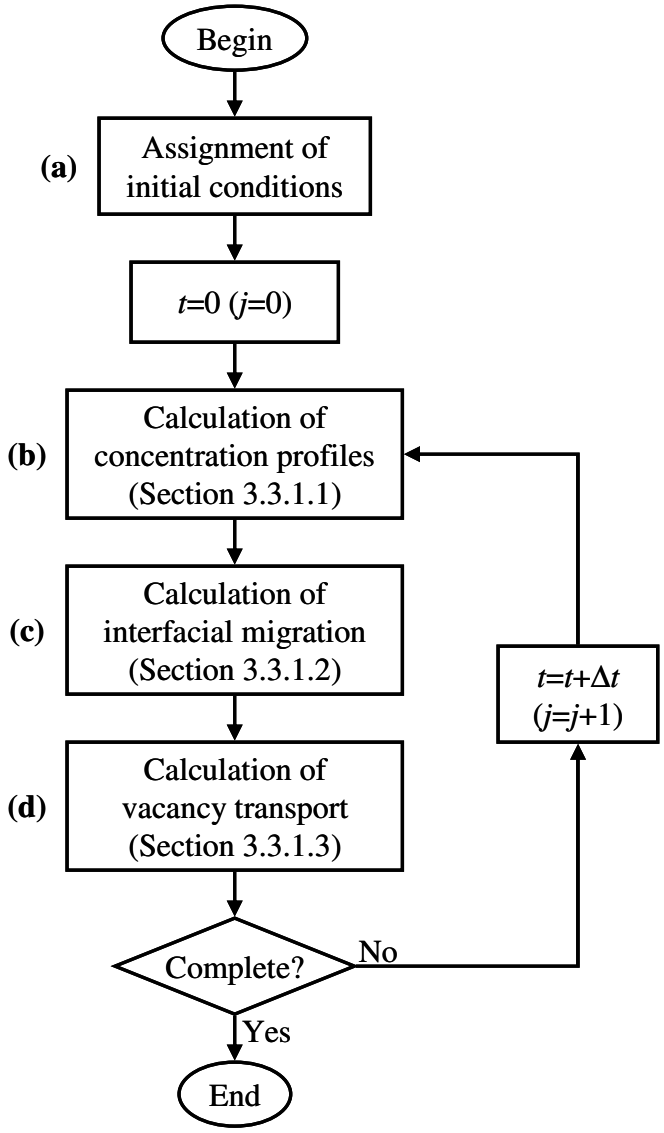


Figure 3.5: Flowchart of the finite difference model

The finite difference method is used in this study to solve the equations presented in the Section 3.3.1. The current enhanced interdiffusion (Section 3.3.1.1) is addressed first because it generates the concentration profile, which in turn controls both the interfacial migration and the vacancy transport. Section 3.3.2.1 first describes the finite differencing in a domain with time constant boundaries. Section 3.3.2.2 describes the modification to this method in order to account for the moving interfaces in this problem.

3.3.2.1 Interdiffusion in a Domain with Time Constant Boundaries

The most intuitive scheme is to describe the solution space as a plane of the time domain t and the spatial domain x. Figure 3.6 shows the uniformly meshed solution space and the corresponding grid and nodes. The spacing in spatial-domain meshing is h, and k is the spacing in time-domain meshing. The running indices are i for the spatial domain and j for the time domain. The yellow nodal points describe the concentration at a given location ($x = ih$) at a given time ($t = jk$) within the phase in question. The green nodal points represent the initial condition ($j = 0$) and their values can be assigned based on Equation (3.20). The red nodal points are the boundary conditions ($i = 0$ or $i = n$), which are constants based on the solubility limits measured on the phase diagram.

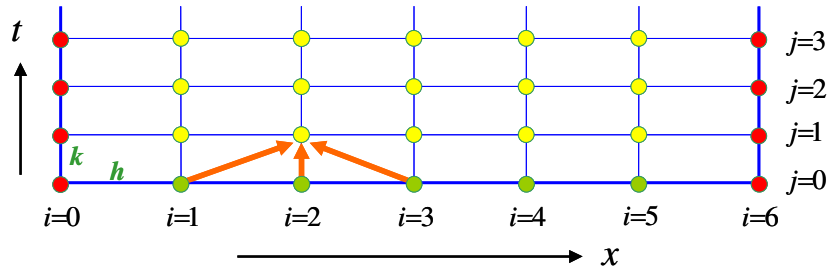


Figure 3.6: Grid and mesh nodes in a finite difference model in a time constant solution. (The arrows indicate functional relationships during the finite difference calculations.)

In Equation (3.19), a second-order derivative is the highest spatial derivative and first-order is the highest time derivative. These can be expressed in an explicit finite difference approximation as follows [3.14]:

For spatial-domain derivatives

$$\frac{\partial^2 w}{\partial x^2} \approx \delta_h^2 w = \frac{1}{h^2}\left(w_{i+1,j} - 2w_{ij} + w_{i-1,j}\right)$$

$$\frac{\partial w}{\partial x} \approx \delta_h w = \frac{1}{2h}\left(w_{i+1,j} - w_{i-1,j}\right) \tag{3.25}$$

where w is the concentration. For the time-domain derivative,

$$\frac{\partial w}{\partial t} \approx \Delta_k w = \frac{1}{k}\left(w_{i,j+1} - w_{ij}\right) \tag{3.26}$$

Substituting the equations above into Equation (3.19), gives:

$$w_{i,j+1} = f\left(w_{i-1,j}, w_{ij}, w_{i+1,j}\right) \tag{3.27}$$

This means that the value of each node can be calculated from the corresponding node and the directly adjacent nodes of the previous iteration. The orange arrows in Figure 3.6 indicate this functional relationship. These arrows begin at the independent variable (known input) and end at the dependent variable (unknown output). Therefore, one can easily show that all unknowns (yellow nodes) at the first iteration ($j = 1$) can be obtained if the initial conditions (green nodes) and boundary conditions (red nodes) are

given. Using information from the previous time-row and the boundary conditions, this calculation is repeated for each new time-row until the objective time is reached. This scheme can provide a solution to the current enhanced interdiffusion equation in a fixed spatial domain.

3.3.2.2 Interdiffusion in a Domain with Time Varying Boundaries

Within the bulk of each phase, the current enhanced interdiffusion can be solved using the method described in the previous section. Nevertheless, some modification is required for the solution in the vicinity of the moving interfaces in order to account for the time-varying spatial domain. This section describes how the moving interphase boundaries are treated in this model. Figure 3.7 shows the diagram of the solution space in the vicinity of a moving interface. The diagram consists of two phases, α and β, and an interface that separates them. The two phases, α and β, can be any two neighboring phases in the diffusion couple. The space is first meshed with fixed spacing of h and k in the spatial domain and time domain, respectively. The fixed nodes, blue and yellow nodes, represent the local concentration within a given phase. They have constant positions, but describe variable concentrations. The blue nodes represent the concentration in the α phase and the yellow nodes in the β phase. The running indices of the concentration nodal arrays for α and β phases are i_α and i_β, and j is the running index for the time-rows.

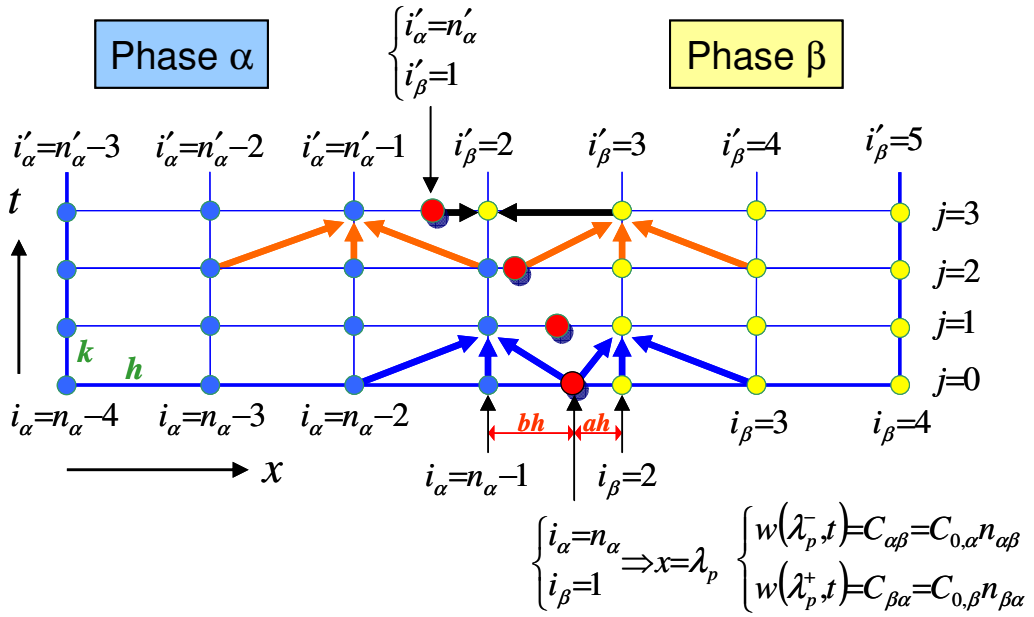


Figure 3.7: Grid and mesh nodes in a finite-difference model in a time-varying solution space. (The arrows indicate functional relationships during the finite difference calculations.)

In addition to the fixed mesh nodes, time-variable nodes, red nodes, are inserted into the solution space and represent the moving interfaces. They have variable positions, λ_p, but constant concentrations that are the solubility limits of the given phases, $C_{\alpha\beta}$ and $C_{\beta\alpha}$. The running index p for the interface λ_p and the interface concentrations are consistent with those shown in Figure 3.1. This means that the red node is a double node which belongs to both α and β phases. For the α phase, it is the last node in the array $i_\alpha = n_\alpha$ and its concentration is the low solubility limit in α, that is $C_{\alpha\beta}$. For the β phase, it is the first node $i_\beta = 1$ and is the high solubility limit in β, that is $C_{\beta\alpha}$. For example, let α be Cu_3Sn and β be Cu_6Sn_5. As shown in Figure 3.1, the interface will be λ_2. Therefore, the red node will have a concentration of C_{23} in the Cu_3Sn phase calculation and a concentration of C_{32} in the Cu_6Sn_5 phase calculation, and its position will be λ_2.

First, consider the case in which the moveable node moves between two adjacent fixed nodes and does not move across either of them. This is the situation for the time-rows $j = 0 \rightarrow j = 1$, as shown in Figure 3.7. The nodal derivative calculation is identical to the description provided in Section 3.3.2.1, where the location is at least one node away from the interface. For the direct neighbors of the interfaces, the finite difference derivatives must be modified, because the three corresponding nodes are no longer uniformly spaced in the previous time-row, as shown in Figure 3.7.

If ah is the distance between the interface node and its right neighbor and bh is the distance between the interface node and its left neighbor, then the finite difference term can be modified as follows. The proof is shown in Appendix C.

In α phase at the left side of the interface,

$$\begin{aligned}
\frac{\partial^2}{\partial x^2} w^{\alpha}_{n_\alpha-1,j} &\approx \frac{2}{h^2}\left[\frac{1}{1+b} w^{\alpha}_{n_\alpha-2,j} - \frac{1}{b} w^{\alpha}_{n_\alpha-1,j} + \frac{1}{b(1+b)} w^{\alpha}_{n_\alpha,j}\right] \\
\frac{\partial}{\partial x} w^{\alpha}_{n_\alpha-1,j} &\approx \frac{1}{h}\left[-\frac{b}{1+b} w^{\alpha}_{n_\alpha-2,j} - \frac{1-b}{b} w^{\alpha}_{n_\alpha-1,j} + \frac{1}{b(1+b)} w^{\alpha}_{n_\alpha,j}\right]
\end{aligned} \tag{3.28}$$

In β phase at the right side of the interface,

$$\begin{aligned}
\frac{\partial^2}{\partial x^2} w^{\beta}_{2,j} &\approx \frac{2}{h^2}\left[\frac{1}{a(1+a)} w^{\beta}_{1,j} - \frac{1}{a} w^{\beta}_{2,j} + \frac{1}{1+a} w^{\beta}_{3,j}\right] \\
\frac{\partial}{\partial x} w^{\beta}_{2,j} &\approx \frac{1}{h}\left[-\frac{1}{a(1+a)} w^{\beta}_{1,j} + \frac{1-a}{a} w^{\beta}_{2,j} + \frac{a}{1+a} w^{\beta}_{3,j}\right]
\end{aligned} \tag{3.29}$$

Based on these equations and the approximation detailed in Appendix C, the interdiffusion can be calculated for nodes adjacent to the interfaces. The finite difference of each node depends on its corresponding node in the previous time row and on its two neighbors. This is shown by the blue arrows in Figure 3.7.

However, a new complication arises when the interface nodes move across the fixed nodes. This is the situation for the time rows $j = 2 \rightarrow j = 3$ in Figure 3.7, which shows an interface node moving across one fixed node to the left. As a result, the array of the left phase α loses its second to last node, whereas the array of the right phase gains an additional node. Note that the first and the last nodes of each phase are always the interface or boundary nodes and the phases never lose these nodes.

When cross-node movement occurs, the calculation of the critical nodes is shown by the orange arrows in Figure 3.7. For the α phase, $i'_\alpha = n'_\alpha - 1$ can be calculated using a standard finite difference as described by Equation (3.25). For the β phase, $i'_\beta = 3$ requires an irregularly spaced finite difference described by Equation (3.29). The additional node in the β phase cannot be obtained using finite difference because it has changed phase since the previous time-row. However, that node can still be calculated by interpolation between the interface node and $i'_\alpha = 3$, which is indicated by the black arrows in Figure 3.7. During the simulation, interface movement was controlled to advance in steps smaller than 1/1000 of the mesh spacing (h) for each time iteration. Hence, the loss of accuracy that was incurred by interpolation was very small.

3.3.2.3 Interfacial Migration

As indicated in Section 3.3.1.2, the calculation of the interfacial migration requires the calculation of the concentration gradients in the vicinity of the interface. Based on the domain meshing shown in Figure 3.7, forward and backward differences are

applied to the spatial-domain derivatives to calculate the concentration gradients in the vicinity of the interface.

$$\frac{\partial}{\partial x} w_\alpha \left(\lambda_p^-, t\right) \approx \frac{1}{(b+1)h}\left(C_{\alpha\beta} - w^\alpha_{n_\alpha - 2, j}\right)$$

$$\frac{\partial}{\partial x} w_\beta \left(\lambda_p^+, t\right) \approx \frac{1}{(a+1)h}\left(w^\beta_{3, j} - C_{\beta\alpha}\right) \tag{3.30}$$

Finally, the time-domain derivative is expressed as follows.

$$\frac{d\lambda_p}{dt} \approx \Delta_k \lambda_p = \frac{1}{k}\left(\lambda_{p, j+1} - \lambda_{p, j}\right) \tag{3.31}$$

3.3.2.4 Vacancy Transport

As indicated in Section 3.3.1.3, first and second derivatives of the concentration are required to calculate the vacancy transport. They have been established in Equation (3.25) for the bulk and in Equations (3.28) and (3.29) for the vicinity of the interfaces.

3.3.3 Simulation Model

The numerical simulation was programmed using Matlab 6.5 and the algorithms described in Section 3.3.1 and 3.3.2. The spatial domain was uniformly meshed with a spacing of 25 nm. At the boundaries of each phase, an extra moveable node was attached in order to represent the moving boundary. The fixed nodes had constant positions and variable concentrations, while the moveable nodes had variable positions and constant concentrations. Figure 3.8 shows the nodal arrays and the moving interface nodes.

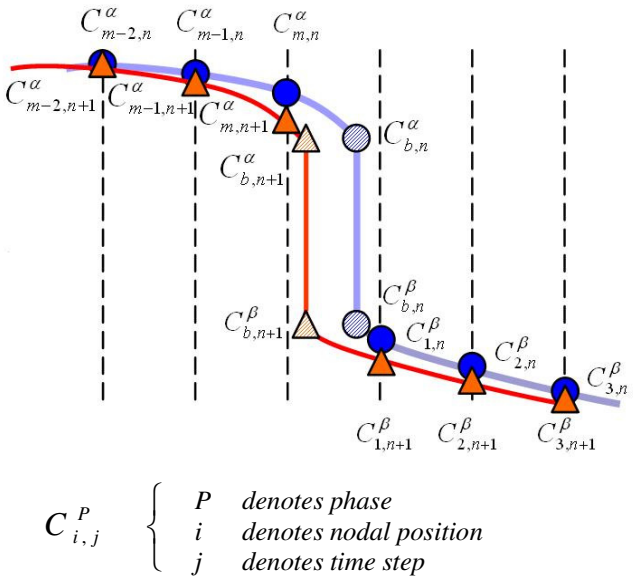


Figure 3.8: Nodal arrays and moving interfacial nodes

The equations in Section 3.3.1.1 were applied in each phase. The boundary conditions are listed in Table 3.1. In dealing with the cladding interfacial nodes and their first and second adjacent nodes, partial differences were adopted as described in Section 3.3.2.2. Once the concentration profile of each phase was obtained, migration of interfaces was determined using Equation (3.23) based on the local concentration gradient at the interfaces. Forward and backward differences were used to calculate the concentration gradients at the interfaces. Current density is an adjustable parameter in this program and can be set to zero to investigate the kinetics of the intermetallic growths that result from thermal aging alone. Discussion regarding the mesh sensitivity and model stability is presented in Section 5.2 because they depend on the parameters used in the model, which will be deduced in Chapter 4.

Chapter 4: Electromigration Parameters

4.1 INTRODUCTION

The equations needed to study interdiffusion and electromigration in a Cu-Sn diffusion couple were described in Chapter 3. To the author's knowledge, no closed-form solution has been proposed for these coupled equations. Accurately simulating these phenomena requires knowledge of the diffusion coefficients and the effective charge numbers of Cu and Sn in each phase. Some of these parameters have been reported in literature whereas the others have not. Section 4.2 first reviews the parameters that are available in the literature. It is proposed in this chapter that the other parameters can be deduced from experimental data describing the intermetallic growth. Section 4.3 describes the methodology used for determination of these parameters. Section 4.4 describes an uncertainty estimation of these deduced parameters.

4.2 MODELING PARAMETERS

The basic assumption of the interdiffusion equation is that each diffusing species must be assigned its own unique and independent diffusivity. The same rule is applied to the effective charge number, the measure of the propensity of a species to be influenced by the external electric field. In the investigation of the kinetics in the Cu-Sn diffusion couple, sixteen independent parameters appear in the governing equations. These are discussed in the following sections.

4.2.1 Diffusion Coefficients

Table 4.1 lists the diffusion coefficients of interest and their temperature dependence as reported in the literature [4.1-4.10]. The temperature dependence of diffusion coefficients can be expressed by the Arrhenius relationship:

$$D(T) = D_0 \exp\left(-\frac{Q}{RT}\right) \tag{4.1}$$

where D is the diffusion coefficient, D_0 is the intrinsic diffusivity of the material, Q is the activation energy for diffusion, R is the gas constant and T is the temperature in degree Kelvin.

The coefficients of self-diffusion in pure Cu and pure Sn are readily available in American Society for Metals (ASM) handbooks and diffusion handbooks [4.1-4.3]. Tin has been shown to have a tetragonal crystal structure [4.11] and its anisotropic diffusion coefficients have been reported [4.3]. Dyson *et al*. [4.4] noted that the mobility of Cu in a pure Sn phase is extremely rapid and anisotropic due to its fast diffusion by an interstitial mechanism.

The diffusion coefficients of Cu and Sn atoms in intermetallic compounds are not well documented. However, the interdiffusion coefficients of the Cu-Sn intermetallic compounds have been reported by a number of research groups. Both Mei *et al*. [4.6] and Onishi and Fujibuchi [4.7] deduced the interdiffusion coefficients by conducting annealing experiments and developing analytical models based on the experimental data. Although the intrinsic diffusivities and activation energies that the two groups deduced were different, their results were reasonably consistent at the temperature of interest.

Table 4.1: Diffusion coefficients in literature

Type of Diffusion	D_0 (m^2/s)	Q (kJ/mol)	D(25°C) (m^2/s)	D(150°C) (m^2/s)	Condition	Ref
$D_{Cu\ in\ (Cu)}$	3.4×10^{-5}	195.6	1.84×10^{-39}	2.44×10^{-29}		[4.1]
	$6.0\text{-}7.8\times10^{-5}$	211.4-213.1	4.51×10^{-42}	4.35×10^{-31}		[4.2]
$D_{Sn\ in\ (Sn)}$	1.2×10^{-9}	43.89	2.45×10^{-17}	4.59×10^{-15}		[4.1]
	7.70×10^{-4}	107.1	1.33×10^{-22}	4.64×10^{-17}	//c	[4.3]
	1.07×10^{-3}	105	4.31×10^{-22}	1.17×10^{-16}	⊥c	[4.3]
$D_{Cu\ in\ (Sn)}$	2.4×10^{-7}	33.02	3.94×10^{-13}	2.01×10^{-11}	⊥c	[4.4]
			$\sim2\times10^{-10}$		//c	[4.4]
$D_{Sn\ in\ (Cu)}$	2.95×10^{-5}	177.0	2.89×10^{-36}	4.18×10^{-27}		[4.5]
	4.1×10^{-7}	129.8	7.46×10^{-30}	3.89×10^{-23}		[4.2]
$\tilde{D}_{Cu_3Sn}$	5.48×10^{-9}	61.86	7.97×10^{-20}	1.27×10^{-16}		[4.6]
	1.43×10^{-8}	70.6	6.12×10^{-21}	2.76×10^{-17}		[4.7]
	3.2×10^{-6}	83.91	6.38×10^{-21}	1.40×10^{-16}		[4.8]
	5.3×10^{-8}	66.1	1.39×10^{-19}	3.67×10^{-16}	Thin film	[4.9]
	8.08×10^{-7}	81.6	4.09×10^{-21}	6.83×10^{-17}	Single Crystal	[4.9]
$\tilde{D}_{Cu_6Sn_5}$	1.84×10^{-9}	53.92	6.58×10^{-19}	4.06×10^{-16}		[4.6]
	1.55×10^{-8}	64.8	6.88×10^{-20}	1.55×10^{-16}		[4.7]
			$>10^{-21}$		Thin film (no Cu_3Sn)	[4.10]

Dreyer *et al*. [4.8] used differential scanning calorimetry to investigate the energetics and kinetics of interdiffusion of solder/metal diffusion couples and the interdiffusion coefficient of Cu_3Sn was alternatively derived. Nevertheless, individual diffusivities of Cu and Sn atoms are required for this study and these have not been reported in the literature to the best of this researcher's knowledge.

4.2.2 Effective Charge Numbers

The electromigration driving force is described by a dimensionless parameter, the effective charge number Z^*. Equation (1.2), derived by Huntington [4.12], is rewritten here as Equation (4.2).

$$F_{eff} \equiv eZ^* E = e\left(Z^e + Z^w\right)E \tag{4.2}$$

The electrostatic charge number Z^e represents the direct electrostatic force on a moving ion and hence its value is expected to be the nominal valence of the ion. The electron wind charge number Z^w accounts for the electron wind force which is generally the dominant contribution. Table 4.2 lists the values of the effective charge numbers of interest [4.13-4.15, 4.17, 4.18].

Table 4.2: Effective charge numbers in literature

Species	Phase	Z^*	References
Cu	Cu	2~7	[4.13-4.15]
	Sn	0.6~3.25 (Pb)	[4.17]
Sn	Cu	---	
	Sn	18	[4.18]

Self electromigration has been reported for both Cu and Sn and their effective charge numbers have been determined [4.13-4.16]. However, the effective charge numbers for Cu and Sn as dilute solutes in each other has not been reported. Hsieh and Huntington [4.17] reported the effective charge number for Cu as a dilute solute in pure Pb. The value fell in the range of 0.6~3.25. The electron wind charge number Z^w of Cu in Pb and in Sn is expected to be similar, since Pb and Sn are both quadrivalent metals in group IV with similar electronic configurations, and Cu atoms diffuse interstitially in both host metals. Therefore, the effective charge number of Cu in pure Pb is considered herein to be similar to that in pure Sn, with reservation. As for the Cu-Sn intermetallic compounds, their effective charge numbers have not been reported.

According to Equations (3.2) and (3.3), calculation of the electromigration induced fluxes requires knowledge of the resistivity of each phase in addition to the effective charge numbers. The resistivity of each phase of interest is listed in Table 4.3.

Table 4.3: Resistivity of the phases in Cu-Sn diffusion couple

Phases	Cu	Cu_3Sn	Cu_6Sn_5	Sn
Resistivity (Ω-nm)	16.8	89.3	175	115
References	[4.19]	[4.20]	[4.20]	[4.19]

4.2.3 Deduced Parameters

Table 4.4 indicates the availability of parameters in the literature. Table 4.4 only indicates whether or not data are available for the parameters of interest. Their values are presented in Tables 4.1 and 4.2.

Table 4.4: Availability of necessary parameters documented in the literature

Species	Parameters	(Cu)	Cu_3Sn	Cu_6Sn_5	(Sn)
Cu	D	[4.1-4.2]	None	None	[4.4]
	Z^*	[4.13-4.15]	None	None	None
Sn	D	[4.2, 4.5]	None	None	[4.1, 4.3]
	Z^*	None	None	None	[4.18]

Note: The values are reported in Table 4.1 and Table 4.2, if available.

As indicated in Table 4.4, at least ten out of the sixteen parameters do not have reported values for use in the kinetic model. For the intermetallic compounds, the only reported parameters are the interdiffusion coefficients (see Table 4.1), which describe the combined effect of both Cu and Sn atoms. However, as discussed in Section 3.2.1, each

atomic species must be given its own intrinsic diffusion coefficient. To the best of this researcher's knowledge, the individual diffusion coefficients of Cu and Sn in the Cu-Sn intermetallic compounds have not been reported in the literature. This discovery is not unexpected, because it is rather difficult to obtain direct measurements of diffusion behaviors for these intermetallic compounds. Measurement of the diffusivity or effective charge number requires placement and detection of diffusion marker. However, these intermetallic compounds exist between the Cu-Sn diffusion couple as thin films or in an irregular morphology. Under conditions in which migration of the diffusion markers can be measured, there is also a strong driving force, which causes these compounds to grow substantially.

Therefore, an approach has been formulated in this study based on the simulated annealing technique that, in conjunction with compound kinetic modeling, allows determination of the parameters of these intermetallic compounds. The experimental data have been taken from the thermal aging work of Siewert *et al.* [4.21] and the electromigration work of Chae [4.22]. These experiments were discussed in Chapter 2.

4.3 DERIVATION OF PARAMETERS USING SIMULATED ANNEALING

4.3.1 Inverse Problems

In an overview, Tarantola [4.23] described inverse problems in the following manner. *Consider the study of a physical system. The model parameters represent the minimal set of parameters that completely describe the system. Forward modeling is the prediction of the observable parameters given values of these model parameters. Inverse modeling is to infer the values of the model parameters according to actual measurements of the observable parameters.*

From a broad perspective, determination of any parameter is a process of solving an inverse problem based on the theorized behaviors of a given system. The *model parameters* are deduced by matching the prediction of a presumptive *governing equation* (model) with the actual *observables* (measured quantities). In this study, the diffusivities and the effective charge numbers are the model parameters to be derived. The intermetallic compound growths are used as the observables. Many reports [4.10, 4.16, 4.22, 4.24-4.27] have agreed that solid-state intermetallic compound growth is induced by interdiffusion during thermal aging and enhanced by the electromigration driving force under current stressing. The equations given in Section 3.3.1 are appropriate governing equations for the growth of intermetallic compounds. Therefore, with the model parameters, observables, and equations clearly identified, the remaining question is whether there is an effective mathematical method through which the parameters can be obtained. It is proposed in this dissertation that they can be obtained using the simulated annealing method. Simulated annealing is a statistical optimization technique that can provide solutions to inverse problems that are difficult to formulate or *ill-posed*. The uncertainty of the solution is an essential question due to the use of a statistical optimization scheme in solving the complex inverse problem. Section 4.4 describes the approach used to provide an answer to this question.

4.3.2 Simulated Annealing

Simulated annealing, proposed by Kirkpatrick *et al*. [4.28], is a Monte Carlo algorithm that draws an analogy between the process of physical annealing and the mathematical problem of finding the global minimum of a function in which local minima may be present. It was originally developed to solve combinatorial optimization problems in many-body systems. A classic example of its application in microelectronics

can be found in IBM's chip performance optimization study, which focused on interconnect routing and circuit placement design [4.29]. In this current study, simulated annealing is employed to deduce the parameters from experimentally observed intermetallic compound growths under various current stressing conditions. A brief description of the approach is given below, and the detailed procedures and results are presented in the following sections.

The first step is to determine the ranges in which the true values of the objective parameters are likely to reside. An arbitrary set of parameters is generated within these prescribed ranges. Predictions for the intermetallic compound growth are then made by applying these parameters to the flux-driven kinetic model. The predictions are compared with the experimental observations (truths) and an objective function is applied to measure the discrepancies. New parameter sets are randomly generated until the optimum parameters, with which the predictions best fit the observations, are found.

In this approach, the model parameters are treated as variables, and the objective function is designed so that its functional value reaches the minimum when the predicted behaviors match the observations. Therefore, model parameters are inferred by finding the set of parameters with which the objective function reaches its global minimum in the solution space. The search range of each parameter is described in Section 4.3.2.1. Section 4.3.2.2 describes the experimental observations and the model predictions. Section 4.3.2.3 describes the objective function that has been designed to measure the discrepancies between the observations and the predictions. Section 4.3.2.4 describes the simulated annealing procedure.

4.3.2.1 Model Parameters

The model parameters to be deduced include the diffusion coefficients D and the effective charge numbers, Z^*, of Cu and Sn atoms in the intermetallic compounds, Cu_3Sn and Cu_6Sn_5. As indicated in Table 4.4 diffusion coefficients and effective charge numbers have been reported in the literature for the two boundary phases, Cu under-bump metallization and Sn solder with the exception of the effective charge number of Cu atoms in the Sn phase and that of Sn atoms in the Cu phase.

In general, if values of a parameter have been reported, the search range is between 0.5 orders of magnitude above and below the reported values. If the parameter has been reported in different sources, the more recent data are used. The ranges for the diffusion coefficients of the intermetallic compounds are between five orders of magnitude above and below the reported interdiffusion coefficients. This is also an intermediate range for the fast diffusion of a Cu atom in pure Sn phase and a Sn atom in pure Cu phase. As to the effective charge numbers, if no value has been reported in the literature, a generic range of 0.1 to 100 is used. The search ranges are given below.

<u>Cu Under-Bump Metallization</u>

D_{Cu}	Reported range	4.35×10^{-31} m^2/sec [4.2]
	Program range	1.38×10^{-31} m^2/sec ~ 1.38×10^{-30} m^2/sec
D_{Sn}	Reported range	4.18×10^{-27} m^2/sec [4.5]
	Program range	1.32×10^{-27} m^2/sec ~ 1.32×10^{-26} m^2/sec
Z^*_{Cu}	Reported range	2 ~ 7 [4.13-4.15]
	Program range	4.5 (Constant)
Z^*_{Sn}	Reported data	No data
	Program range	0.1 ~ 20

Intermetallic Compounds (Cu_3Sn and Cu_6Sn_5)

D_{Cu}	Reported range	No data
	Program range	1.00×10^{-20} m^2/sec ~ 1.00×10^{-10} m^2/sec
D_{Sn}	Reported range	No data
	Program range	1.00×10^{-20} m^2/sec ~ 1.00×10^{-10} m^2/sec
Z^*_{Cu}	Reported range	No data
	Program range	0.1 ~100
Z^*_{Sn}	Reported data	No data
	Program range	0.1 ~ 100

Sn Solder

D_{Cu}	Reported range	2.01×10^{-11} m^2/sec [4.4]
	Program range	6.36×10^{-12} m^2/sec ~ 6.36×10^{-11} m^2/sec
D_{Sn}	Reported range	4.64×10^{-17} m^2/sec [4.3]
	Program range	1.47×10^{-17} m^2/sec ~ 1.47×10^{-16} m^2/sec
Z^*_{Cu}	Reported range	0.6 ~ 3.25 (for Cu atoms in Pb) [4.17]
	Program range	0.1 ~10
Z^*_{Sn}	Reported data	18 [4.18]
	Program range	18 (Constant)

4.3.2.2 Observations and Model Predictions

The intermetallic compound growth is used as the experimental observables from which the diffusion and electromigration parameters are to be inferred. Although the goal of this study is to investigate the electromigration effect, knowledge of aging data is

critical to the deduction of the parameters. The drift velocity due to electromigration depends on the product of the effective charge number and the diffusion coefficient. Therefore, it is not possible to determine these two parameters separately given only electromigration data. Aging kinetics is only related to diffusivity; thus, decoupling of these two parameters is possible if the aging data are available.

Observations

The experimental results from which the parameters are inferred are presented in Sections 2.3 and 2.4. The intermetallic compound growth data based on thermal aging are shown in Figure 2.1. The data for electromigration are shown in Figure 2.3.

Model Predictions

The model predictions for intermetallic compound growth are calculated using Equation (3.23) based on arbitrary parameter sets generated using the simulated annealing technique. A fast evaluation of Equation (3.23) is required because the model predictions must be repeated many times. Therefore, the kinetic model is simplified by assuming that the concentration profiles of the intermetallic compounds are linear. Figure 4.1 shows the difference that can result in the calculation of concentration gradient. The example depicts the left interface of the Cu_6Sn_5 phase. In the finite difference model, no linear assumption is made and the concentration profile depends on the interdiffusion and electromigration conditions, as indicated by the blue curve. Therefore, in this case, the local concentration gradient, $\theta_{f.d.}$, can be calculated in the vicinity of the interface. If a linear concentration profile is assumed, as indicated by the red line, the concentration gradient, θ_{lin}, is calculated by dividing the range of concentration by the intermetallic compound thickness. The finite difference model is

more accurate, but the linear assumption provides the fast evaluation that is desired by the simulated annealing approach. The deduced parameters were subsequently applied to the finite difference model and found to be valid. This will be discussed in Section 5.2.3.

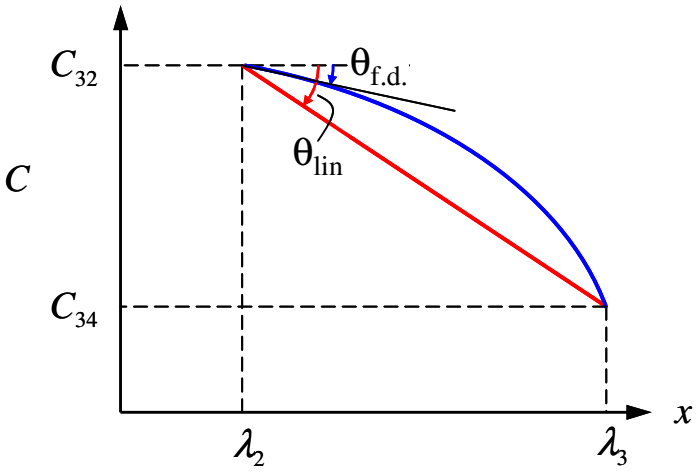


Figure 4.1: Difference in the calculation of the concentration gradient near the interface. (This example diagram is for Cu_6Sn_5, as part of Figure 3.1)

With the assumption of a linear concentration profile, Equation (3.23) now becomes:

$$\lambda_p(t) = \lambda_p^0 + \int_{t_0}^{t} \left(\bar{a} \frac{C_{p,p+1} - C_{p,p-1}}{\lambda_p - \lambda_{p-1}} + \bar{b} \frac{C_{p+1,p+2} - C_{p+1,p}}{\lambda_{p+1} - \lambda_p} + \bar{c} \right) dt \tag{4.3}$$

The numerical integration in Equation (4.3) can be expressed as follows.

$$\lambda_p^m = \lambda_p^0 + k \sum_{j=0}^{m-1} \left(\bar{a} \frac{C_{p,p+1} - C_{p,p-1}}{\lambda_p^j - \lambda_{p-1}^j} + \bar{b} \frac{C_{p+1,p+2} - C_{p+1,p}}{\lambda_{p+1}^j - \lambda_p^j} + \bar{c} \right) \tag{4.4}$$

Therefore, the model prediction of the intermetallic compound thickness at a given time is expressed as:

$$\delta_p = \lambda_p^m - \lambda_{p-1}^m \tag{4.5}$$

where m specifies the time-row of the given time when the experiment observation was obtained. The phase numbering, as shown in Figure 3.1, is indicated by p.

4.3.2.3 Objective Function

The objective function in this study measures the discrepancy between the observed data and the corresponding prediction made with a given set of model parameters. The optimum model parameters can therefore be deduced by finding the minimum in the objective function. Equation (4.6) describes the objective function and Figure 4.2 provides an example of how the discrepancy is calculated.

$$S(\Psi) = \frac{1}{N} \sum_s \sum_p \left\{ \sigma_s \left[\frac{\delta(\Psi, t_s)}{d_s} \right]^2 \right\} \tag{4.6}$$

where N is the total number of observables, s is the running index for the individual observable (intermetallic compound thickness), p indicates the phase, $\delta(\Psi,t_s)$ is the discrepancy between experimental observations and the model prediction obtained with Equation (4.5), Ψ is the model parameter set, t_s is the time of observation, d_s is the intermetallic compound thickness observed at time t_s, and σ_s is the weight parameter.

The objective function $S(\Psi)$ is dimensionless because the discrepancy, $\delta(\Psi,t_s)$ is normalized to the observed thickness, d_s. Each observation can be assigned its individual

weight parameter, σ_s, if necessary. However, in this study, σ_s is set to one for all observations. This objective function is semi-infinite. When all model predictions match the observations exactly, $S(\Psi)$ reaches the minimum, which is zero. There is no upper limit for this objective function because the model predictions can deviate significantly from the observations when improper parameters are used. If all model predictions deviate from the observations for 100% of the observed values, $S(\Psi)$ will be one. Therefore, when the parameter search approaches the truth, the values of $S(\Psi)$ are expected to be between zero and one.

In addition to least squares, other powers were considered, for example, the power of one (linear) and the power of three. However, no additional advantage has been found to be associated with the use of higher or lower powers in the objective function.

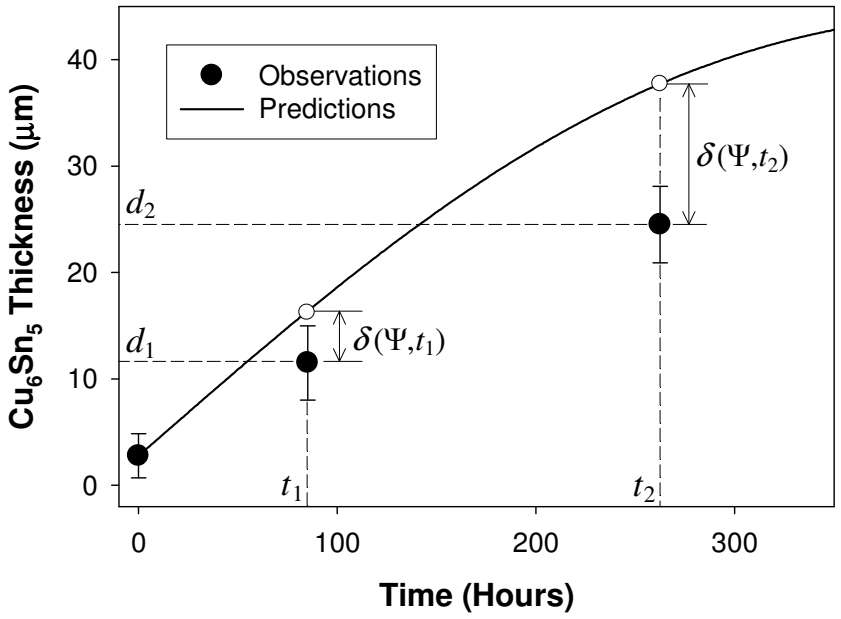


Figure 4.2: The objective function measures the discrepancy between the model predictions and the experimental observations (Ψ is an arbitrary parameter set with which the model prediction is generated)

4.3.2.4 Algorithm

This procedure has been programmed in Microsoft Visual Studio 2005 using the ANSI C language. Figure 4.3 shows the flow chart of the simulated annealing algorithm used in this study, which is described here. The simulation starts from a random state, that is, a random parameter set, Ψ_A, is obtained. All model parameters are chosen randomly in the predetermined range, as indicated in Section 4.3.2.1. In the simulated annealing process, the nominal temperature, Θ, slowly decreases from the "melting temperature," Θ_m, to the "freezing temperature," Θ_f, according to the annealing schedule to be described in Section 4.3.2.5. In each iterative step, one parameter, p_i, is randomly picked, and a step size, Δp_i, is randomly chosen. The chosen parameter, p_i, then attempts to make a move to $\pi_i = p_i + \Delta p_i$ of the random step size. This generates a new parameter set, Ψ_B. The objective function, Equation (4.6), is calculated based on the current state and the attempted new state of the system. The acceptance probability for the change from the current state to the new state is based on the famous Metropolis criterion [4.30].

$$P_{AB} = \min\left(1, \exp\left(\frac{S(\Psi_A) - S(\Psi_B)}{\Theta}\right)\right) \tag{4.7}$$

where P_{AB} is the probability of acceptance of the transition from current state A to the new state B, $S(\Psi)$ is the objective function in Equation (4.6), Ψ is the model parameter set, and Θ is the nominal temperature. Because the objective function $S(\Psi)$ is dimensionless, the nominal temperature Θ must also be dimensionless. A discussion regarding Θ is presented in Section 4.3.2.5.

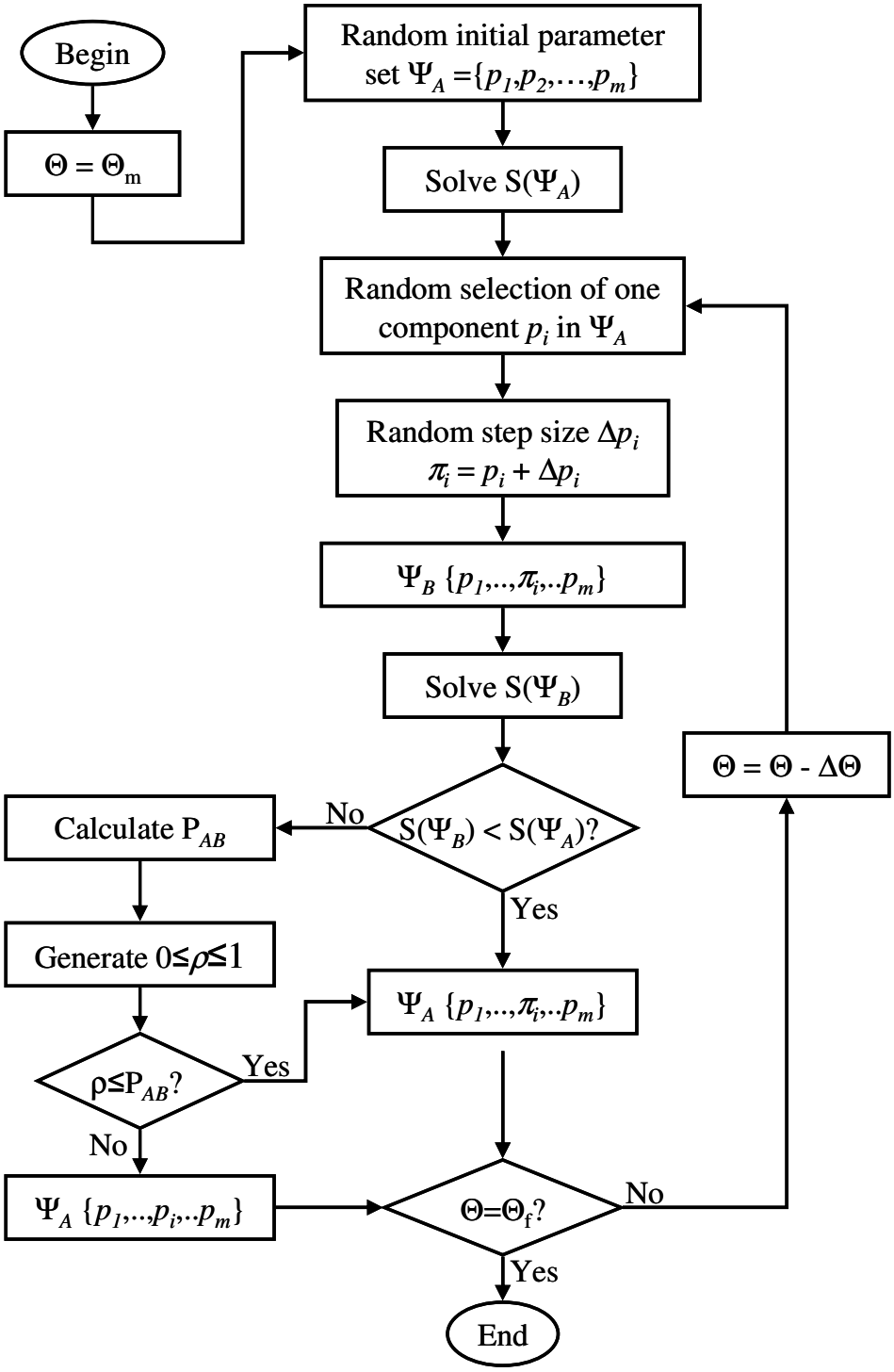


Figure 4.3: Flow chart of the simulated annealing algorithm

The energy of the current state A is $S(\Psi_A)$, and the energy of the new state B is $S(\Psi_B)$. If $S(\Psi_B) < S(\Psi_A)$, that is, the new state B provides a better fit between the predictions and the observations, then $P_{AB} = 1$ according to Equation (4.7), and this attempted move will be accepted. However, if $S(\Psi_B) > S(\Psi_A)$, that is, the new state B provides a worse fit, then $P_{AB} < 1$, and this attempted move will be accepted or rejected based on probability. The acceptance probability is P_{AB}. In this case, an additional random number ρ between zero and one is generated. If $\rho < P_{AB}$, the move will be accepted, otherwise, the move will be rejected. If the move is accepted, the system state becomes $S(\Psi_B)$. If the move is rejected, the system state remains $S(\Psi_A)$. After the decision is made, the system begins the next iteration cycle. The use of the Metropolis criterion allows the system to escape from local minima with the use of probability.

A periodic boundary condition is applied to the range of each parameter to ensure its full exploration during the simulation. It is important to note that the diffusion coefficients and the effective charge numbers are modeled in different manners. The effective charge number Z^* should be modeled in a linear space because a generic range of 0.1 to 100 is more than enough to describe its solution space. In contrast, the solution spaces of the diffusion coefficients span many orders of magnitude; therefore they are modeled in a logarithmic space in order to maintain equal resolution within each order.

4.3.2.5 Annealing Schedule

To simulate the physical annealing process, the nominal temperature, Θ, is gradually decreased from the "melting temperature," Θ_m, to the "freezing temperature," Θ_f. As described earlier, the nominal temperature and the objective function are both dimensionless. The value of Θ_m in this study is one, which is comparable to the objective function value of significant discrepancy from truth, that is, a 100% deviation for all

model predictions. Therefore, $\Theta_m = 1$ is sufficient to allow the system to escape from the local minima. The value of Θ_f is determined by trial and adjusted so that the acceptance probability of the unfavorable moves is below 0.05% toward the end of the simulation. The results of this study have been obtained with $\Theta_f = 10^{-6}$, and have been produced using the exponential annealing schedule shown in Figure 4.4.

The initial 5% of the schedule has an equilibrium at Θ_m. The nominal temperature is then decreased exponentially to Θ_f, followed by an equilibrium at Θ_m in the final 5% of the schedule. Linear annealing schedules have also been tried, however, the exponential schedules have been found to be more effective. The optimum parameters are approached after progressing approximately 70% of the way through the schedule. This does not happen with a linear annealing schedule with the same Θ_m and Θ_f until progressing over 90% of the way through the schedule.

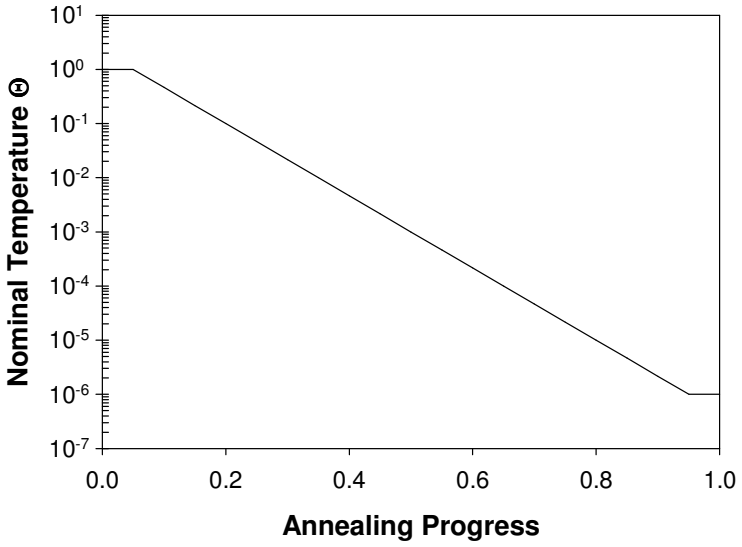


Figure 4.4: Annealing schedule ($\Theta_m = 1$, $\Theta_f = 10^{-6}$)

4.3.3 Results and Discussions

Table 4.5 shows the diffusion coefficients and effective charge numbers deduced with the simulated annealing technique for both Cu and Sn atoms in the intermetallic compounds of Cu_3Sn and Cu_6Sn_5. Since the diffusion coefficients of the individual species in the Cu-Sn intermetallic compounds have never been reported, there are no values available from the literature with which to directly compare them. However, Mei *et al*. [4.6], Onishi and Fujibuchi [4.7], and Dreyer *et al*. [4.8] reported the interdiffusion coefficients which describe the combined effect of Cu and Sn diffusivities in the intermetallic compounds. The diffusion coefficients of individual species are related to the interdiffusion coefficients through Equation (3.10). The highest and lowest values reported for the interdiffusion coefficients are listed in Table 4.5 for reference.

Table 4.5: Deduced diffusion coefficients and effective charge numbers

Phase	Species	Z*	D (m^2/s)	Interdiffusion coefficient (m^2/s)	Interdiffusion coefficient *literature* (m^2/s)
Cu_3Sn	Cu	30	9.2×10^{-16}	6.3×10^{-16}	*2.87×10^{-17}[4.7]~ 3.81×10^{-16}[4.9]*
	Sn	32	5.3×10^{-16}		
Cu_6Sn_5	Cu	21	1.8×10^{-15}	1.3×10^{-15}	*1.61×10^{-16}[4.7]~ 4.19×10^{-16}[4.5]*
	Sn	21	9.6×10^{-16}		

Note: The effective charge numbers are rough estimates. The estimation of solution uncertainty is discussed in Section 4.4.

As parameters have been deduced using simulated annealing, the literature values for the interdiffusion coefficients have not been used in the program. However, the interdiffusion coefficients based on the deduced diffusion coefficients have been found to be consistent with the literature results, as shown in Table 4.5. Therefore, this provides a preliminary verification and an indication that the diffusion coefficients obtained in this study are reasonable. Further discussion regarding the deduced parameters will be presented in Section 4.3.3.1 (diffusion coefficients) and Section 4.3.2.2 (effective charge numbers).

As has been noted, most parameters of the boundary phases, Cu under-bump metallization and Sn solder, have been reported in the literature; their values are provided in Tables 4.1 and 4.2. In the simulated annealing process, these parameters are allowed to vary in the vicinity of the reported values, as indicated in Section 4.3.2.1, in order to improve the fit, since there are variances in the data reported by different sources. Table 4.6 lists the values of these parameters when the optimum fit has been achieved. They are shown here for reference and to demonstrate that the values used for the optimum fit are very similar to those reported when the parameters of the intermetallic compounds were obtained.

Table 4.6: Parameters of Cu under-bump metallization and Sn solder used in optimum fit

Species	Phase	Diffusion Coefficients (m^2/sec)		Effective Charge Number	
		Fit	Literature	Fit	Literature
Cu	Cu-UBM	4.5×10^{-31}	4.35×10^{-31} [4.2]	4.5 (Constant)	2 ~ 7 [4.13-15]
	Sn solder	1.5×10^{-11}	2.01×10^{-11} [4.4]	0.5	0.6 ~ 3.25 (in Pb) [4.17]
Sn	Cu-UBM	4.4×10^{-27}	4.18×10^{-27} [4.5]	18	Not reported
	Sn solder	2.0×10^{-17}	4.64×10^{-17} [4.3]	18 (Constant)	18 [4.18]

Note: For reference only

4.3.3.1 Diffusion Coefficients

As indicated in Table 4.5, the diffusion coefficients of Cu and Sn in the intermetallic compounds have been found to be within one order of magnitude of each other. It has been argued that diffusion in highly ordered intermetallic compounds occurs via more complex mechanisms because the simple nearest-neighbor jump of a vacancy inevitably leads to disordering of the atomic structure. The concept of correlated nearest neighbor vacancy jumping that maintains the atomic ordering was first proposed for the B2 atomic structure by Elcock and McCombie [4.31] and Huntington *et al.* [4.32] and is called the six-jump cycle (6JC) or the Huntington-McCombie-Elcock (HME) mechanism. The structure of a B2 compound constitutes two interpenetrating simple-cubic sublattices, which the two component elements of the alloy occupy respectively. The immediate result of the correlated jump mechanism is strong coupling between the component

diffusion coefficients of the intermetallic compounds. Bakker [4.33] indicated that the 6JC mechanism imposes limits on the ratio of the component diffusivities as follows:

$$0.5 < D_A^* / D_B^* < 2 \tag{4.8}$$

where A and B are the two components of the binary alloy and D_A^* and D_B^* are the component tracer diffusion coefficients. Due to experimental errors which inevitably occur, the diffusion coefficients that have been derived in this study are not sufficiently definite to substantiate this relationship. However, the ratios of the component diffusion coefficients (D_{Cu}/D_{Sn}) are 1.7 and 1.9 for Cu_3Sn and Cu_6Sn_5, respectively. The Cu_6Sn_5 structure belongs to a hexagonal NiAs (B8) type cell [4.34]. However, the range of its stoichiometric composition is approximately 0.54 ~ 0.55, which is close to the ideal composition, 0.5, of a B2-type structure. One would therefore expect the component diffusion coefficients of Cu_6Sn_5 to follow a relation similar to Equation (4.8). The D_{Cu}/D_{Sn} ratio obtained for Cu_6Sn_5 in this study appears to be in agreement with the arguments made by Elcock and McCombie [4.31], Huntington *et al.* [4.32] and Bakker [4.33] that correlated vacancy jumps are likely the dominant diffusion mechanism in the intermetallic compounds and that the component diffusivities are very similar.

4.3.3.2 Effective Charge Numbers

Although the effective charge number Z^* measures the strength of the electromigration driving force, the induced diffusive flux is still restrained by the diffusivity of the species in the phase of interest. Drift velocity is controlled by the product of effective charge number and diffusivity, Z^*D. In order to decouple Z^* from D, knowledge of D is required. Therefore, the simultaneous fitting of thermal aging data is

required to anchor the values of the diffusion coefficients in the heuristic search for the optimum values of the effective charge number. The effective charge numbers of Cu have been found to be 30 for Cu_3Sn and 21 for Cu_6Sn_5. The effective charge numbers of Sn have been found to be 32 for Cu_3Sn and 21 for Cu_6Sn_5. The effective charge numbers obtained for the intermetallic compounds in this study are rough estimates. This will be explained in the study presented in Section 4.4.

4.4 SOLUTION UNCERTAINTY ESTIMATION

In this study, the parameters are inferred by the optimization scheme and not by explicit functional relationships. Therefore, one important question arises. *How definite are the parameters so obtained?* Consider the examples shown in Figure 4.5. Assume that Ψ_1, Ψ_2, and Ψ_{opt} are three arbitrary parameter sets generated in the simulated annealing process, and that Ψ_{opt} is eventually determined to be the optimum.

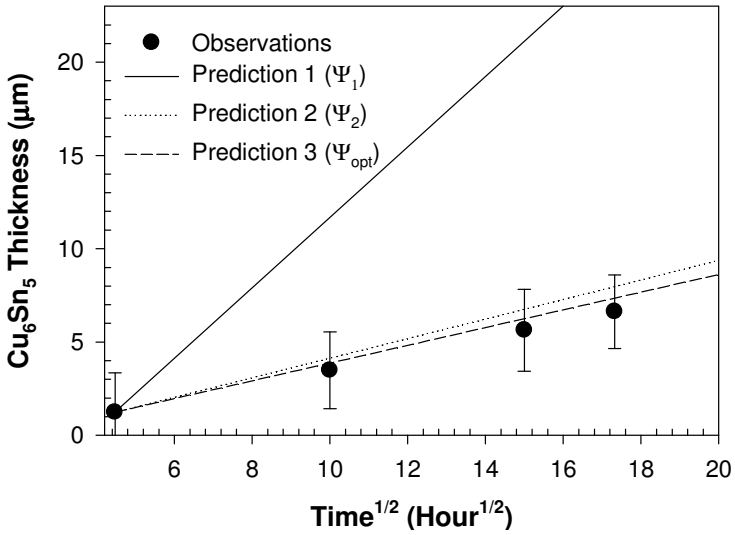


Figure 4.5: The model predictions and the experimental observations (Ψ_1 to Ψ_3 are random parameter sets with which the model predictions were generated; the example shown is Cu_6Sn_5 growth during thermal aging)

In this study, the experimental observations are considered to be truths. As described earlier, Ψ_{opt} are obtained when the cooling rate is sufficiently slow. In Figure 4.5, the model prediction based on Ψ_1 deviates significantly from the observations, and therefore, Ψ_1 is clearly not a valid parameter set. However, it is still possible that there exists a parameter set different from Ψ_{opt}, for example Ψ_2, with which the model also generates reasonable predictions. However, Ψ_2 can never be discovered by simulated annealing. This is because Ψ_2 deviates slightly further from the observations than Ψ_{opt} and simulated annealing always leads the system to its minimum, which is Ψ_{opt}. In order to investigate whether alternative parameter sets are possible, the following study has been conducted.

4.4.1 Concept

The algorithm presented in this section has been deliberately designed to subject the system to a rapid cooling instead of a slow annealing. Although the rapid cooling does not invariably lead the system to the optimum, it is sufficient in insuring the system avoids the regions that are unlikely to provide acceptable solutions. This is because the probability is very low that the system will move to a state that will cause a significant increase in the objective function. In addition, there is a high probability the system will move from a state of high objective function value to a state of lower objective function value. By randomly repeating the rapid cooling procedure many times, the regions in which the objective function values are relatively low can be located. The model predictions for the parameter sets in these regions do not deviate far from the experimental observations. These regions can be further confined by eliminating the regions that cause the prediction to exceed the error bars of the observations.

4.4.2 Procedure

Step 1: Simulated annealing is conducted using a rapid cooling rate. The initial and final nominal temperatures remain the same ($\Theta_m = 1$, $\Theta_f = 10^{-6}$), but the number of steps taken is reduced, as shown in Table 4.7. The parameters of Cu under-bump metallization and Sn solder are not allowed to vary, and the values in Table 4.6 are used.

Step 2: Repeat step 1 for one thousand times.

Step 3: Steps 1 and 2, result in one thousand sets of parameters. The model predictions based on these parameter sets were compared with the experimental observations. If any prediction exceeds the error bars of the observations from the functioning solder joints, that parameter set is excluded.

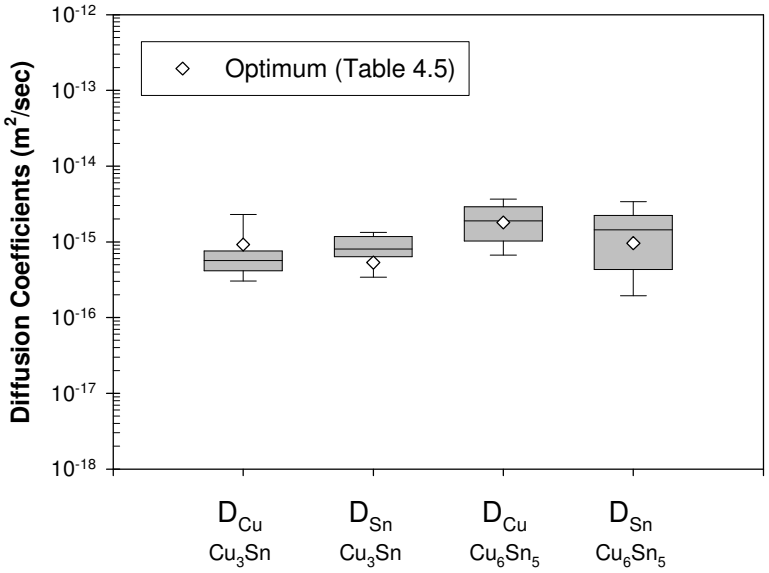
Due to the rapid cooling, the deduced parameters are no longer the optimum and a different parameter set is obtained in each run. As shown in Table 4.7, for the case in which there are 1,000 steps, only 3.5% of the deduced parameter sets generate acceptable predictions, that is, fall within the observation error bars. For the case in which there are 100,000 steps, 28.9% of the deduced parameter sets generate acceptable predictions. The ranges of these acceptable parameter sets are discussed in next section.

Table 4.7: Tests for solution uncertainty estimation

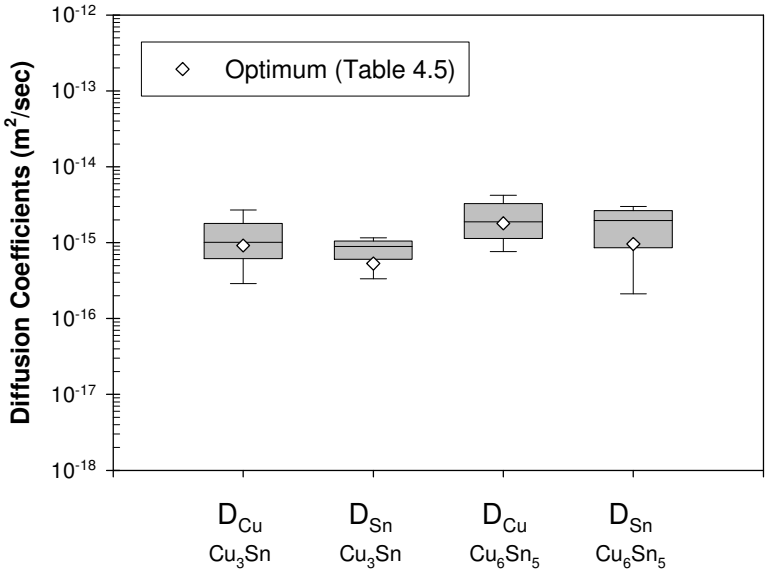
Tests	1	2	3	4	5
Step Number	1,000	3,200	10,000	32,000	100,000
Acceptable Solution	3.5%	14.4%	24.9%	26.1%	28.9%

4.4.3 Results

Figure 4.6 shows the ranges of the diffusion coefficients for Cu_3Sn and Cu_6Sn_5 obtained using the above procedure. The results obtained with 1,000 steps and 100,000 steps are shown in Figure 4.6 (a) and (b), respectively. It is clearly shown in Figure 4.6 (a) that the ranges of diffusion coefficients deduced in this study are approximately within 1 to 1.5 orders of magnitude. When the cooling rate is increased, as shown in Figure 4.6 (b), the determined ranges are still very similar to those in Figure 4.6 (a). The optimum diffusion coefficients are also shown in Figure 4.6. The optimum diffusion coefficients appear to indicate that Cu is the faster diffusing species in both Cu_3Sn and Cu_6Sn_5. However, the analysis in this section shows that it can not be determined in this study whether Cu or Sn has a higher diffusivity because of the significant overlap of the ranges of Cu and Sn diffusivities shown in Figure 4.6.



(a)

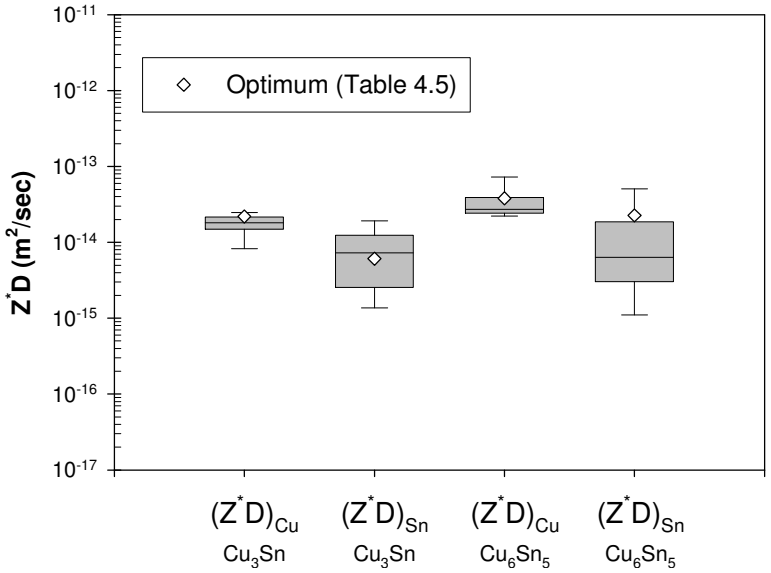


(b)

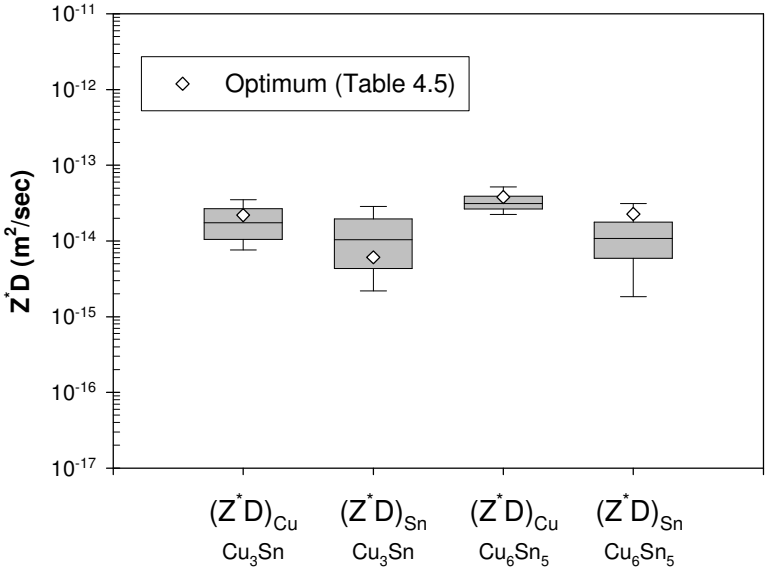
Figure 4.6: Ranges of diffusion coefficients: (a) determined by 1,000 Monte Carlo cooling steps and (b) determined by 100,000 Monte Carlo cooling steps. The error bars indicate the 90th percentile ranks and the boxes indicate the 75th percentile ranks of the valid sets of parameters. Diamonds indicate the optimum parameters reported in Table 4.5.

While the ranges of the diffusion coefficients have been successfully obtained, the ranges of the effective charge numbers, unfortunately, have not. The deduced effective charge numbers do not clearly converge into narrow ranges such as those shown for the diffusion coefficients in Figure 4.6. Therefore, it is concluded that these deduced effective charge numbers are rough estimates, as was explicitly pointed out in Table 4.5 and Section 4.3.3.2. This is due to the difficulty in decoupling Z^* from D when they are obtained simultaneously. The model space of the diffusion coefficients spans ten orders of magnitude, while the model space of 0.1 to 100 is considered sufficient for the effective charge number. Therefore, a definite deduction of the effective charge number requires more definite knowledge of the diffusion coefficients, which is not available for this study.

However, as discussed in Section 4.3.3.2, the drift velocity is in fact controlled by Z^*D (the product of the effective charge number and the diffusion coefficient), rather than controlled solely by the effective charge number Z^*. Therefore, the deduced parameters are still valid for the calculation of electromigration induced fluxes if Z^*D can be determined with a certainty similar to that of the diffusion coefficients. Figure 4.7 shows the ranges of the Z^*D parameters obtained with the two cooling rates described earlier. Z^*D has the same unit as the diffusion coefficient because the effective charge number is a dimensionless parameter. Comparing Figure 4.6 with Figure 4.7, for Cu, the deduced Z^*D have even narrower ranges than the deduced diffusion coefficients. For Sn, the ranges for Z^*D are slightly wider than the corresponding diffusion coefficients. Therefore, this study provides reasonable estimates of the Z^*D parameters which control the electromigration-induced fluxes.



(a)



(b)

Figure 4.7: Ranges of Z^*D, effective charge numbers multiplied by diffusion coefficients, (a) determined by 1,000 cooling steps and (b) determined by 100,000 cooling steps. The error bars indicate the 90^{th} percentile ranks and the boxes indicate the 75^{th} percentile ranks of the valid sets of parameters. Diamonds indicate the optimum parameters reported in Table 4.5.

The range explored above is mainly attributed to the variance in the experimental data and the uncertainty of the fitting approach. Further studies which include more accurate experimental data points under various test conditions are necessary to improve the accuracy of the deduced parameters. Nevertheless, simulated annealing in conjunction with kinetic modeling has been demonstrated to enable the investigation of the diffusion and electromigration parameters using experimentally observed intermetallic compound growths.

4.5 ADVANTAGES OF SIMULATED ANNEALING

This study has utilized the simulated annealing technique to deduce diffusion coefficients and effective charge numbers. The optimum parameter set has been determined using an annealing schedule that utilized ten million Monte Carlo steps. This took approximately thirty minutes of time on a regular PC equipped with a 2.3GHz dual core processor. However, if a brute-force search was to be used with a coarse grid resolution of one order of magnitude, the number of steps required would become 11^{10} and the expected simulation time would be four weeks. If higher resolution is required or more parameters are included, the computation time would increase exponentially. The simulated annealing technique is not restricted by the meshing resolution and it provides significantly higher computation efficiency than the brute-force search approach. Therefore, it is a superior technique for the problem studied in this dissertation, in which many parameters have to be deduced simultaneously.

The minimization of the predetermined objective function does not guarantee that the appropriate solution of a parameter extraction problem has been found. Judgment must be exercised based on knowledge of the material properties of the alloy system of interest. The design of an objective function can also use *a priori* information to anchor certain model parameters and stabilize the solution. However, as a first attack on this problem, no technique of this kind has been employed.

Chapter 5: Simulation in Intermetallic Compound Growth Kinetics and Electromigration-Enhanced Void Formation

5.1 INTRODUCTION

This chapter describes the modeling of the electromigration-enhanced intermetallic compound growth of Pb-free Sn-based solder on Cu under-bump metallization. The model was formulated in Chapter 3. The important parameters were obtained in Chapter 4 based on the experimental data by others as described in Chapter 2.

Due to the non-planar nature of the intermetallic compounds and data variance, the growth laws of the intermetallic compounds are difficult to determine through experiments alone. However, intermetallic compound kinetics has a significant impact on the evaluation of the lifetime of Sn-based Pb-free solders subject to current stressing. This study provides a theoretical investigation of intermetallic compound growth kinetics based on the parameters obtained with experimental results. Void formation is the most dominant failure mode for Pb-free solder joints under electromigration and is controlled by vacancy fluxes [5.1]. Therefore, vacancy transport has also been studied using the intermetallic compound kinetic model. Finally, the kinetic model has been used to study two effects: current density and Cu diffusivity in Sn solder. Study of the current density effect can assist in the design of accelerated electromigration testing to obtain critical results efficiently. Results from the study of the effect of Cu diffusivity in Sn solder can assist in the design of an optimal material to extend the lifetime of solder joints under electromigration.

5.2 MODEL VERIFICATION

This section first describes an investigation of the stability and mesh sensitivity of the model. The validation of the model is then investigated.

5.2.1 Model Stability

Model stability requires that a small perturbation in the data that arises due to approximation remains small in the latter stage of the simulation and that it has minimal effects on the modeling results. For instance, consider the following partial differential equation.

$$\frac{\partial u}{\partial t}=\frac{\partial^2 u}{\partial x^2}, \qquad \text{for } u=u(x,t) \tag{5.1}$$

For fixed-mesh grids, an explicit finite difference approximation of Equation (5.1) can be expressed as

$$u_{i,j+1}-u_{ij}=\frac{k}{h^2}\left(u_{i+1,j}-2u_{ij}+u_{i-1,j}\right) \tag{5.2}$$

In Equation (5.2), h is the mesh spacing in distance, and k is the mesh spacing in time. The explicit method, Equation (5.2), is numerically stable and convergent when the solution is smooth and the following condition is satisfied [5.2].

$$r=\frac{k}{h^2}\leq\frac{1}{2} \tag{5.3}$$

where r is a convergence parameter. In this expression, h should be estimated first, because it depends on the smoothness of u as a function of x at any given time t. For a u that has steep slopes, the meshing needs to be fine (small h). The implication of this criterion is that the time-step size (k) should decrease with the square of the space-mesh size (h) in order to maintain stability. However, reducing r increases the simulation time, because more iteration steps are required.

In this study, Equation (3.13) is the partial differential equation of the highest order. In order to obtain an estimate of the convergence parameter r, the lower order terms are temporarily neglected and Equation (3.13) is rewritten as follows.

$$\frac{\partial C}{\partial t}=\tilde{D}\frac{\partial^2 C}{\partial x^2} \tag{5.4}$$

where C is the concentration of each phase and $\tilde{D}$ is the interdiffusion coefficient. The concentration profile is in the narrow ranges for each intermetallic phase, so $\tilde{D}$ can be treated as a constant in this preliminary estimation. Let c be the discrete solution of C. The finite difference of Equation (5.4) can then be expressed as follows.

$$c_{i,j+1}-c_{ij}=\frac{k}{h^2}\tilde{D}\left(c_{i+1,j}-2c_{ij}+c_{i-1,j}\right) \tag{5.5}$$

Comparing Equation (5.5) and Equation (5.2), it can be shown that the critical criterion for convergence can be rewritten as Equation (5.6).

$$\frac{k}{h^2}\tilde{D}\leq\frac{1}{2} \tag{5.6}$$

The required convergence parameter can therefore be estimated as

$$r=\frac{k}{h^2}\leq\frac{1}{2\tilde{D}_{\max}} \tag{5.7}$$

In Equation (5.7), $\tilde{D}_{\max}$ is the highest interdiffusion coefficient in the Cu-Sn diffusion system. The convergence parameter required for this study can be estimated based on the diffusion coefficients reported in Table 4.5,

$$r\leq 3.8\times 10^{14}\ \text{sec}\cdot m^{-2} \tag{5.8}$$

This estimate has been derived for fixed mesh grids and only accounts for the terms of the highest order in Equation (3.13). In this study, the diffusion problem has been treated with mesh grids that contain moving boundary nodes. Lower-order derivatives in Equation (3.13) that arise from the electromigration-induced flux and treatment of interdiffusion coefficients may also play a role in affecting the model's stability; therefore, additional monitoring steps have been taken in the simulation to insure the convergence of the model solution.

In order to prevent instability, the concentration profiles have been monitored. The program compares the concentration gradients between adjacent elements in the same phase to detect small local perturbations. The model has been programmed to generate warnings when the adjacent elements have gradients of opposite signs, an indicator of a local perturbation. When a warning has been received, the simulation has been conducted again with an incrementally decreased convergence parameter, *r*. It has been found that the criterion in Equation (5.8) is sufficient for the model to achieve

stability in the aging simulation. Lower r values are required for the electromigration simulation. This can be attributed to the higher intermetallic compound growth rates and the lower-order electromigration terms. For the electromigration simulation, the r value required for stability is approximately 2.9×10^{14} sec/m^2. This value has been found by incrementally decreasing r until stability is achieved. However, the results reported in this dissertation have been obtained with an r value that is approximately 25% lower than that required to insure stability.

5.2.2 Mesh Sensitivity

Ideally, the simulation results should be independent of the mesh densities and depend only on the governing equations. In reality, the mesh densities can play a role in the approximation of derivatives and the accuracy of the solution. In order to investigate the mesh sensitivity of the model, simulations have been conducted using identical parameters, but with various mesh densities in time or in distance. These verifying simulations are described as follows.

(1) Baseline

Space-mesh spacing (h): 25 nm

Convergence parameter (r): 2.2×10^{14} sec/m^2

Description: The results of this dissertation have been obtained using this baseline condition.

(2) Doubling mesh density in space

Space mesh spacing (h): 12.5 nm

Convergence parameter (r): 2.2×10^{14} sec/m^2

Description: The density of the space mesh is doubled while the convergence parameter r remains constant. If the space meshing of the baseline simulation is sufficiently fine, the results generated by this simulation should be close to that of the baseline simulation.

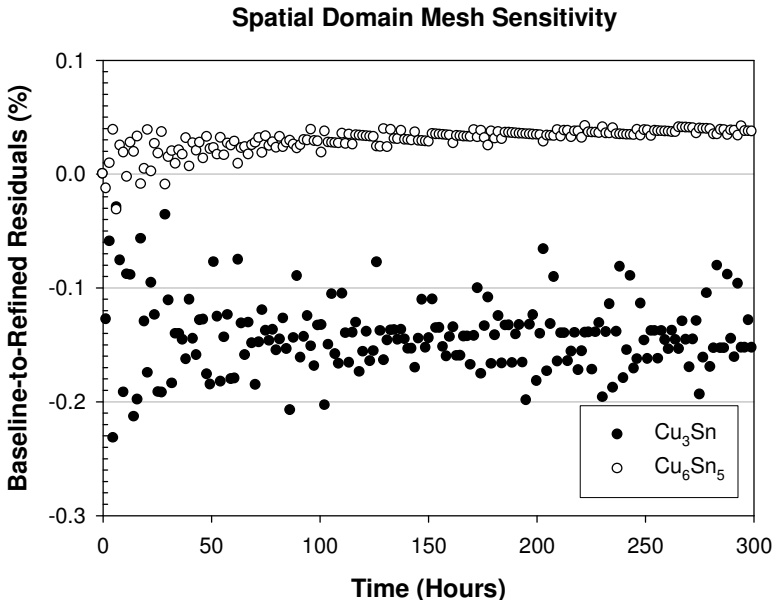
(3) Doubling mesh density in time

Space mesh spacing (h): 25 nm

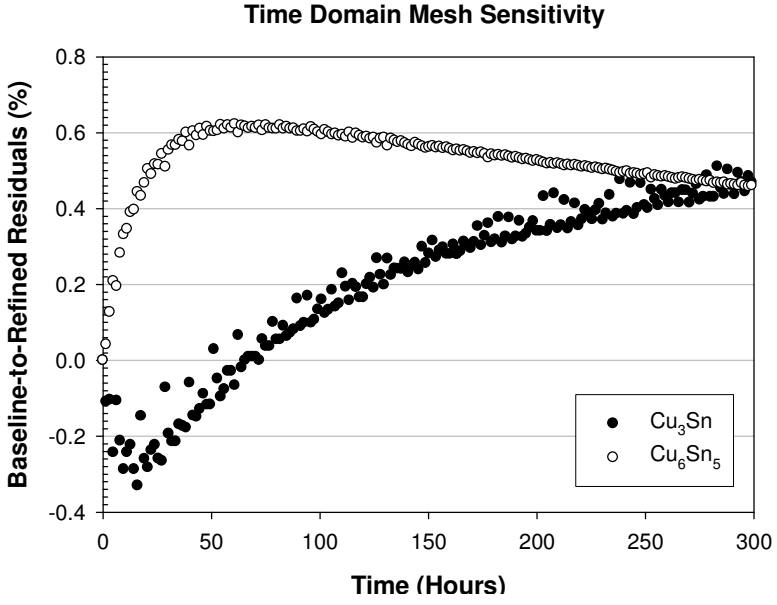
Convergence parameter (r): 1.1×10^{14} sec/m^2

Description: The object of this simulation is to verify the time-step size. By keeping h constant and halving r, the step-size k is halved, that is, the mesh density in time domain is doubled. If the time step of the baseline simulation is sufficiently small, the result generated by this refined simulation should be close to that of the baseline simulation.

These three mesh conditions have been applied to simulate intermetallic compound growth under current stressing of 5.16×10^4 Amp/cm^2, the most demanding case in this study. Figure 5.1 shows the residuals of the solution using the standard mesh to that using the refined mesh. These results indicate that increasing the mesh fineness in time t or in distance x has minimal effect on the numerical solution and, therefore, the mesh densities chosen in this study are appropriate.



(a)



(b)

Figure 5.1: Effect of mesh density on the simulated intermetallic compound thickness under 5.16×10^4 Amp/cm^2 current stressing: (a) Spatial domain mesh refinement and (b) time domain mesh refinement.

5.2.3 Model Validation

Figure 5.2 shows a comparison of the simulation results to experimental observations of the intermetallic compound thickness. Each point represents an experimental observation. All experimental points that were obtained from the aging (Section 2.3) and electromigration (Section 2.4) are presented here and compared with the corresponding model predictions. Figures 5.3 and 5.4 show the comparison of the simulation results to the experimental data for each aging and electromigration condition. The predicted intermetallic compound thickness is fairly consistent with the reported experimental data in aging and electromigration conditions.

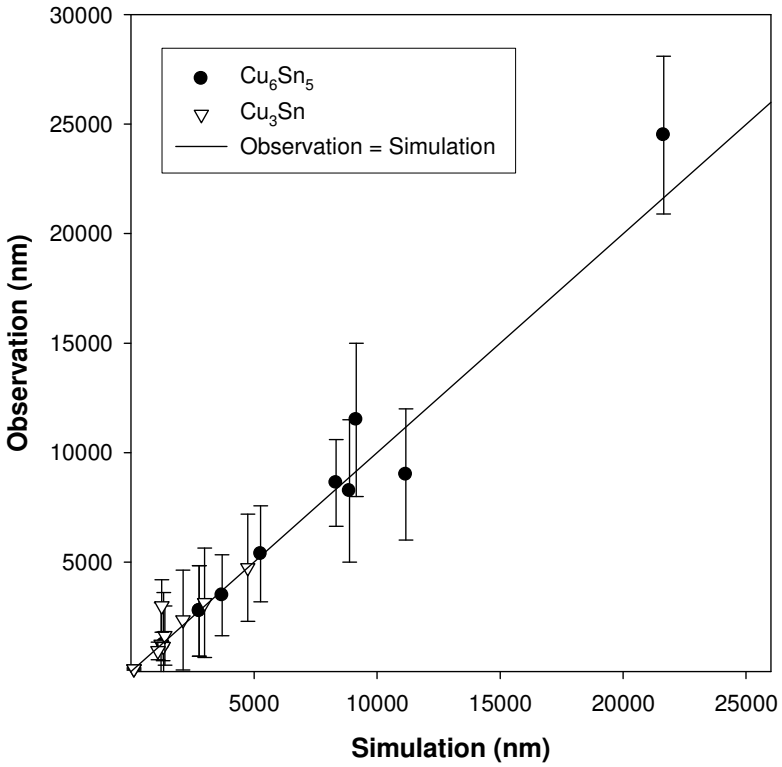


Figure 5.2: Correlation between observations (measurements) and simulation. The measurements were reported by others as described in Section 2.3 (thermal aging experiment) and Section 2.4 (electromigration experiment).

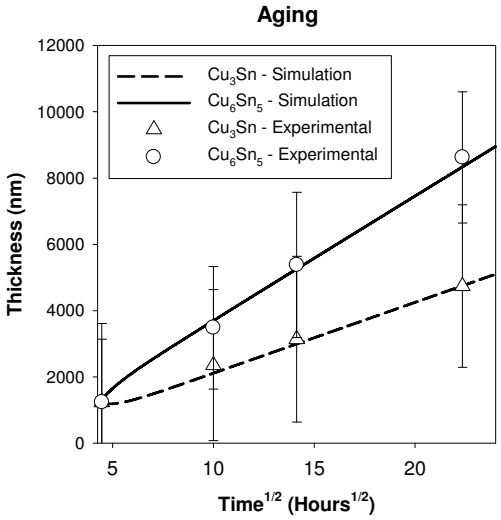
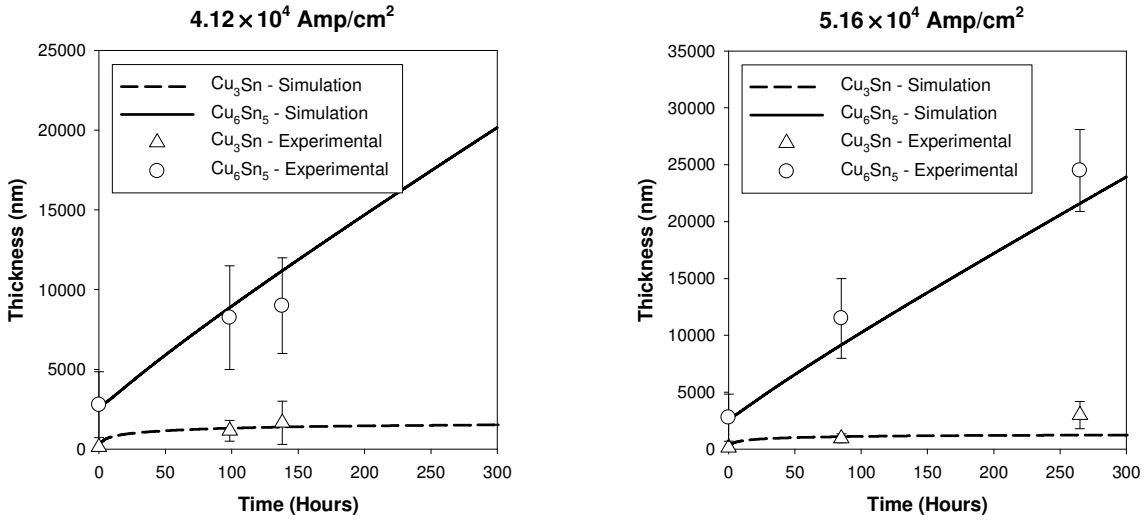


Figure 5.3: Experimental and simulated intermetallic compound growth during thermal aging (Experimental data from T.A. Siewert *et al*. in Ref [5.3])[7]



(a) (b)

Figure 5.4: Experimental and simulated intermetallic compound growth under electromigration: (a) 4.12×10^4 Amp/cm^2, and (b) 5.16×10^4Amp/cm^2 (Experimental data from S.-H. Chae in Ref [5.4])[8].

[7] Contribution of NIST; not subject to copyright in U.S.

[8] With kind permission from S.-H. Chae, Master Report, the University of Texas at Austin, August 2006.

5.3 INTERMETALLIC COMPOUND GROWTH KINETICS

This section describes the theoretical study of the intermetallic compound kinetics using the model formulated in Chapter 3 and the parameters obtained in Chapter 4. The kinetics under thermal aging and under electromigration have both been studied. The results indicate different growth laws for these two conditions.

5.3.1 Thermal Aging

To demonstrate the different kinetics of current induced growth and diffusion controlled growth, an analysis has been conducted for intermetallic growth due to thermal aging ($j = 0$). Figure 5.5 shows the intermetallic thickness as a function of aging time. The current density was set to zero for the aging simulation. The time axes in Figure 5.5 (a) and (b) are linear, and in (c) and (d) are in the square root of time. The intermetallic growth kinetics appear to follow parabolic law in the thermal aging simulation for both Cu_3Sn and Cu_6Sn_5.

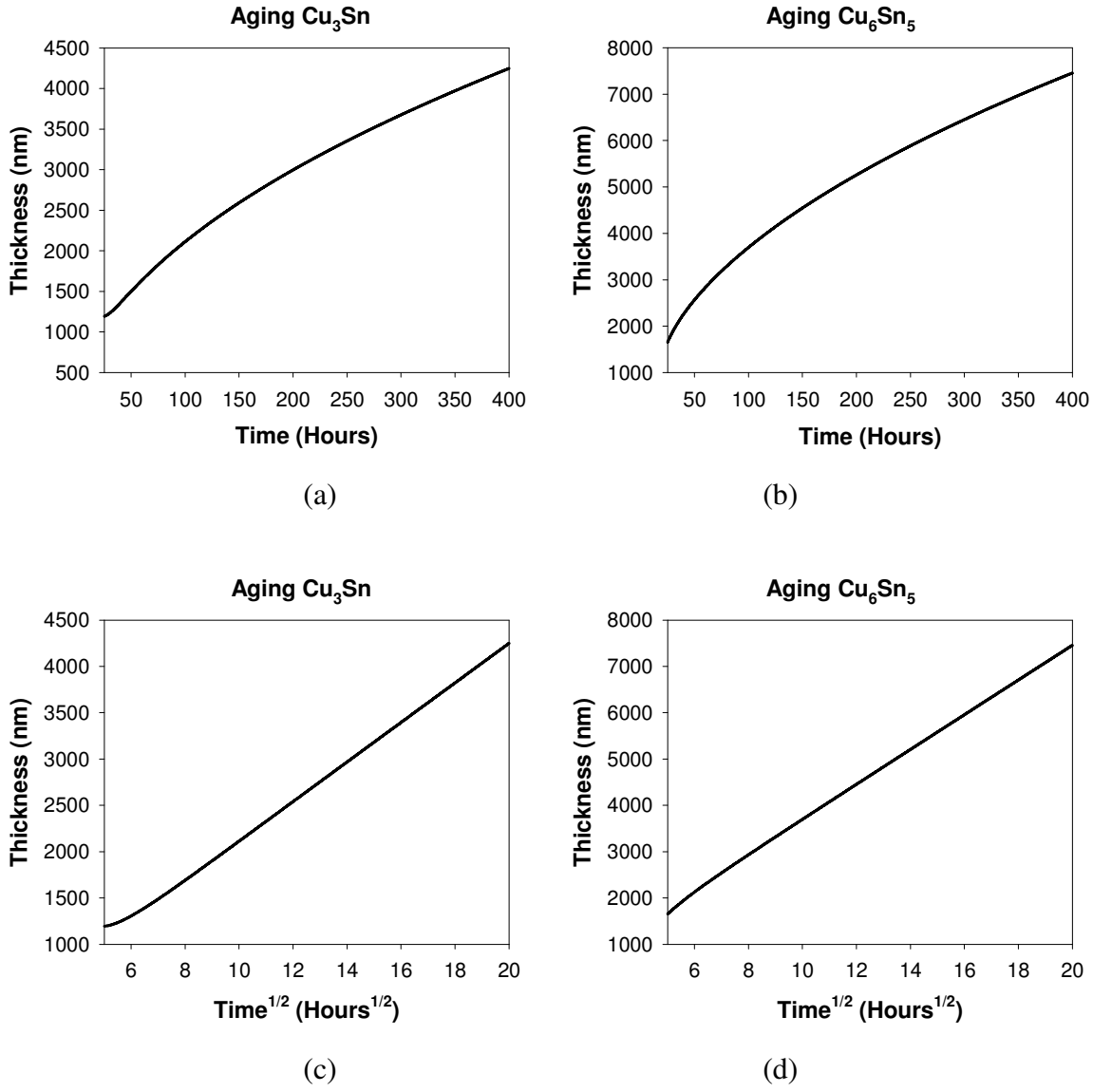


Figure 5.5: Intermetallic compound growth during thermal aging: (a) Cu_3Sn and (b) Cu_6Sn_5 growth plotted against time; and (c) Cu_3Sn and (d) Cu_6Sn_5 growth plotted against the square root of time

5.3.2 Electromigration

Figure 5.6 shows the simulated time dependence of the thickness of Cu_3Sn and Cu_6Sn_5 under current stressing conditions: 4.12×10^4 Amp/cm^2 and 5.16×10^4 Amp/cm^2.

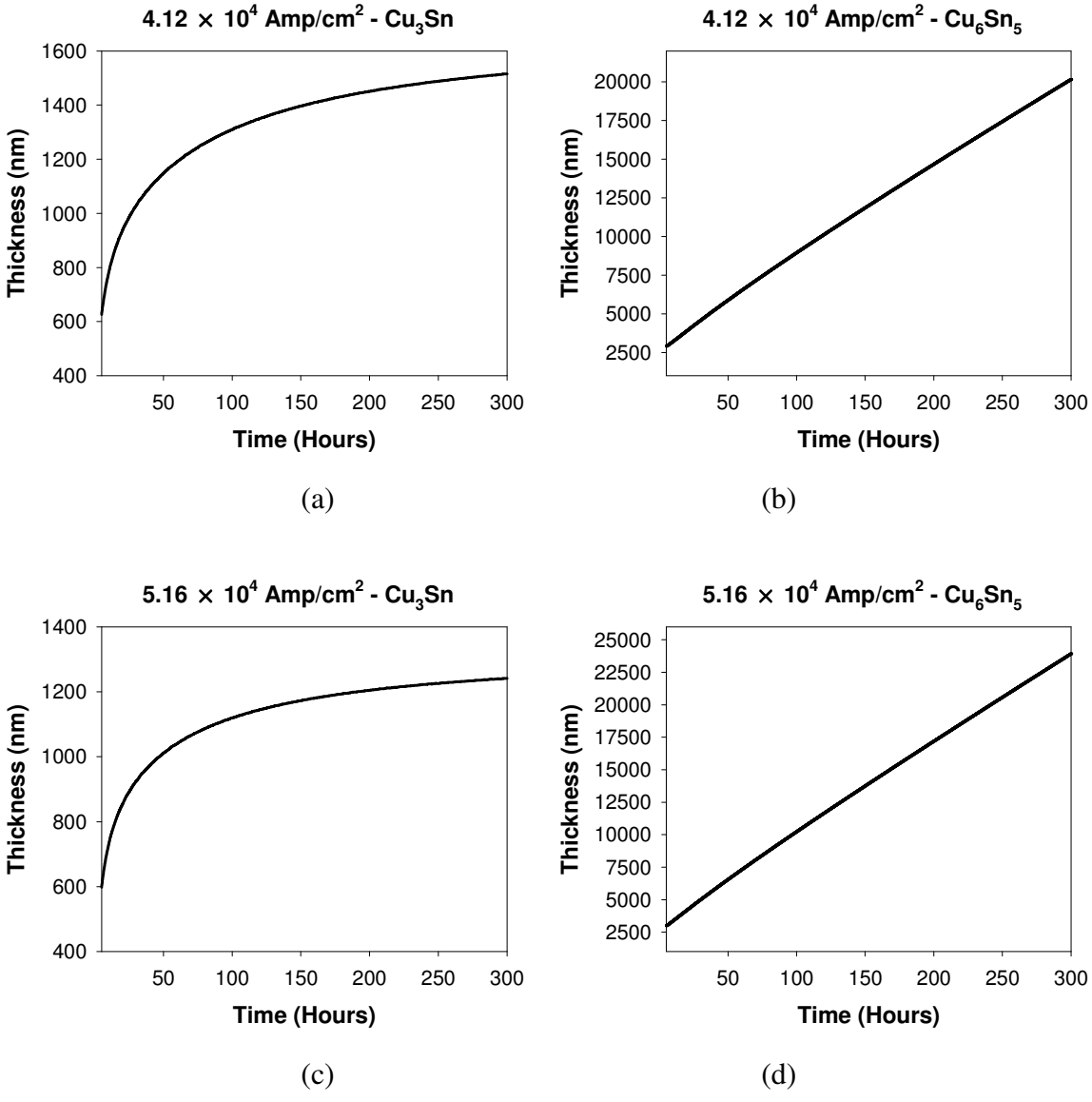
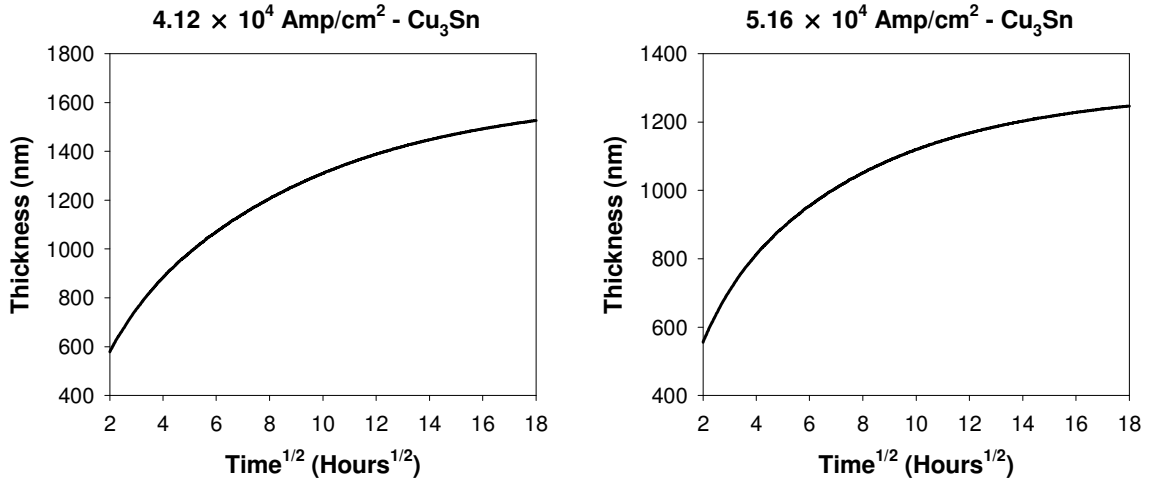


Figure 5.6: Electromigration-enhanced intermetallic compound growth: (a) Cu_3Sn and (b) Cu_6Sn_5 under 4.12×10^4 Amp/cm^2; and (c) Cu_3Sn and (d) Cu_6Sn_5 under 5.16×10^4 Amp/cm^2

The thickening of Cu_3Sn is significantly slower than the thickening of Cu_6Sn_5 in the current stressing simulation, as shown in Figure 5.6. This is consistent with the observation that Cu_3Sn remains a very thin conformal layer between Cu_6Sn_5 and Cu under-bump metallization during the electromigration experiments. According to the model, Cu_3Sn grows at a decaying rate under electromigration, as shown in Figure 5.6 (a) and (c). No straightforward growth law has been found for Cu_3Sn; however, the growth rate clearly decays faster than a $t^{1/2}$ law, as shown in Figure 5.7. On the other hand, the thickening of Cu_6Sn_5 is significantly enhanced by electromigration. For Cu_6Sn_5, the thickening clearly follows a linear law, as shown in Figure 5.6 (b) and (d). The results also indicate that Cu_6Sn_5 is by far the dominant intermetallic compound in the Cu-Sn system under electromigration.



(a) (b)

Figure 5.7: Electromigration enhanced Cu_3Sn growth plotted against the square root of time: (a) 4.12×10^4 Amp/cm^2 and (b) 5.16×10^4 Amp/cm^2

5.3.3 Intermetallic Compound Growth Kinetics

Intermetallic compound growth is the controlling parameter and has significant effects on the reliability of the solder joints. Therefore, understanding the growth laws of the intermetallic compounds is an important undertaking in the evaluation of the solder lifetime. It is difficult to distinguish the linear and parabolic growth laws through experiments alone. This is attributed to the non-planar nature of the intermetallic compounds and the data variances that usually occur in electromigration experiments. However, applying an inappropriate growth law can lead to significant deviation in the projected behavior. This is because the estimation of the lifetime requires extrapolation of experimental results. This work provides a theoretical investigation of intermetallic compound growth kinetics under thermal aging and electromigration. The results of this modeling study indicate the following intermetallic compound growth kinetics.

Thermal aging causes both Cu_3Sn and Cu_6Sn_5 to grow according to a parabolic law. Under electromigration, Cu_6Sn_5 growth is significantly enhanced by current stressing and is by far the dominant intermetallic compound. Electromigration causes Cu_6Sn_5 growth to follow a linear law. The kinetic model also indicates that the other intermetallic compound, Cu_3Sn, grows at a rate that appears to decay faster than a $t^{1/2}$ law. These results indicate that the reliability of the Pb-free solder must take into account the linear growth of Cu_6Sn_5 under aggressive current stressing. This requires a more conservative design rule than one that assumes a parabolic growth law for Cu_6Sn_5. The rapid growth of Cu_6Sn_5 also has significant effects on vacancy transport, which causes the void formation under electromigration.

5.4 ELECTROMIGRATION-ENHANCED VOID FORMATION

The rate of vacancy concentration increase (R) was first calculated using Equation (3.18). Figure 5.8 shows that the simulated R is negative for both Cu_3Sn and Cu_6Sn_5. This means that the vacancies need to be created in order for the equilibrium vacancy concentration to be maintained in these two intermetallic compounds. It is important to note that the vacancy concentration does not necessarily increase or decrease at the rate of the calculated R. The R value should only be considered an estimate of the tendency for vacancies to be created or destroyed at a given location. In this case, Figure 5.8 indicates that vacancies are created in the bulk of the intermetallic compounds.

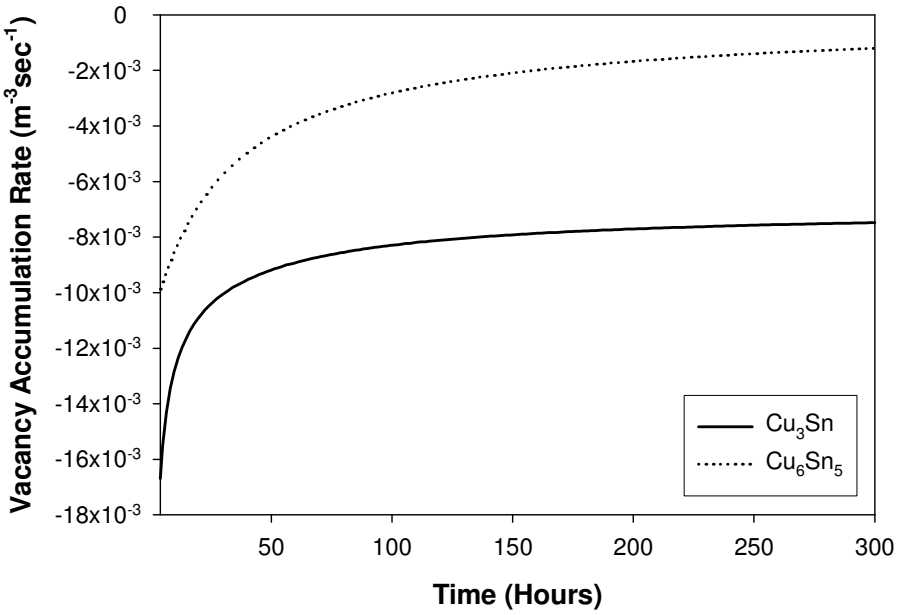
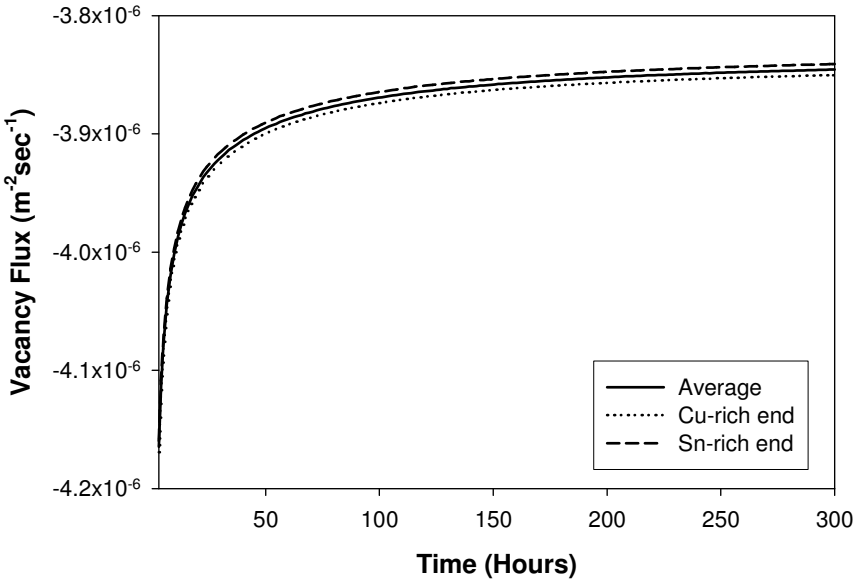


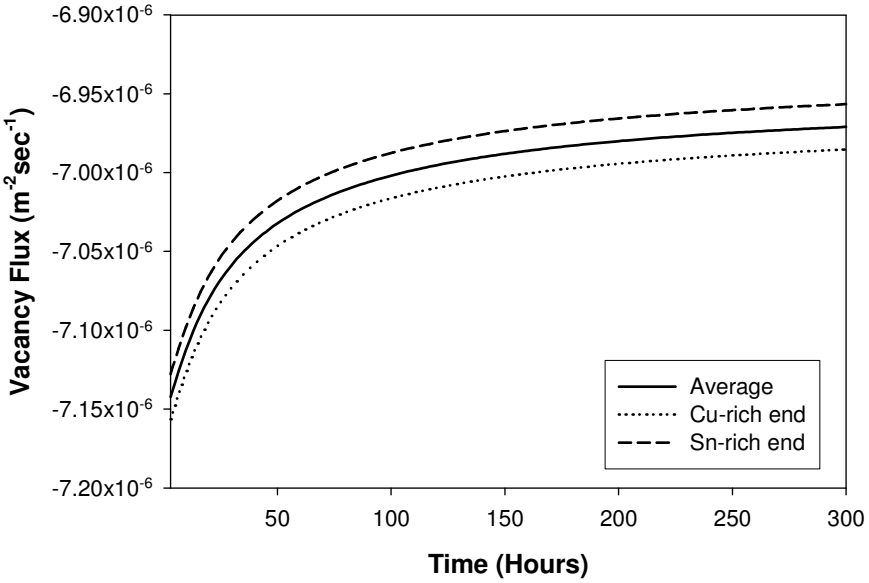
Figure 5.8: The rate at which vacancy concentration increases, if vacancies are not created or annihilated when the solder joint is subjected to 5.16×10^4 Amp/cm^2 current stressing

In order to understand how voids form under current stressing, the vacancy fluxes in the intermetallic compounds have been calculated using Equation (3.6). The results are shown in Figures 5.9 and 5.10. Figure 5.9 (a) and (b) show the vacancy fluxes in Cu_3Sn and Cu_6Sn_5 as functions of the current stressing time. Figure 5.10 (a) and (b) show the vacancy fluxes in Cu_3Sn and Cu_6Sn_5 as functions of the intermetallic compound thickness. The vacancy fluxes calculated at the Cu-rich end and Sn-rich end of the intermetallic compound have been plotted along with the average.

It is clear from these plots that the vacancy fluxes in both Cu_3Sn and Cu_6Sn_5 are negative in value. This indicates that there is a net number of vacancies diffusing from the Sn solder side to the Cu under-bump metallization side. The vacancy flux in Cu_6Sn_5 has also been found to be greater than that in Cu_3Sn because the absolute values of the calculated vacancy flux in Cu_6Sn_5 are higher.

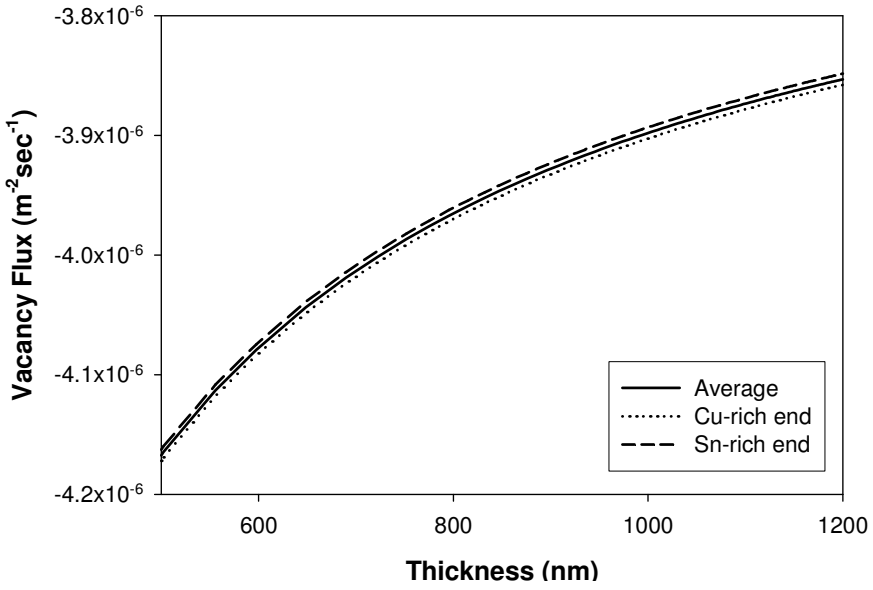


(a)

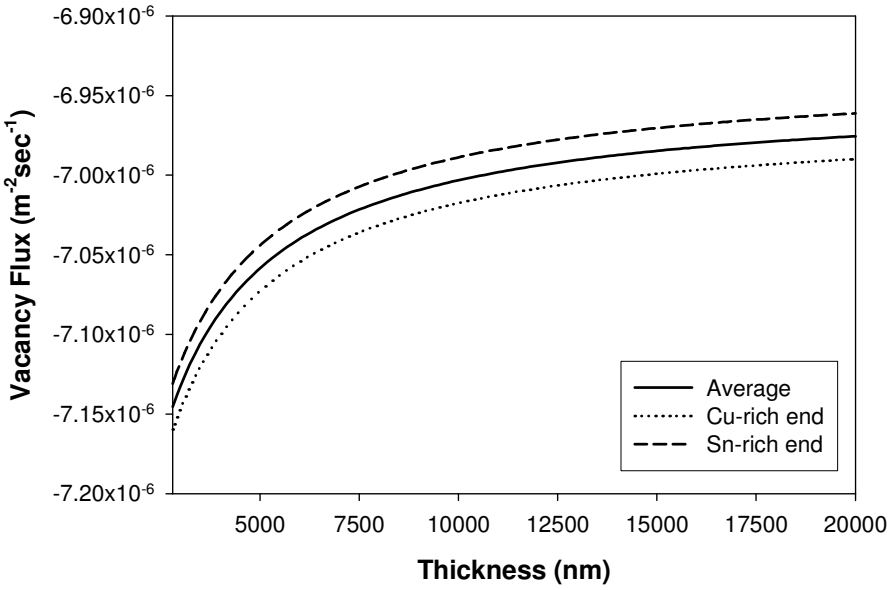


(b)

Figure 5.9: Simulated vacancy flux as a function of current stressing time at a current density of 5.16×10^4 Amp/cm^2: (a) Cu_3Sn and (b) Cu_6Sn_5. (A negative sign indicates that the vacancy flux is moving in the direction from Sn solder to Cu under-bump metallization)



(a)



(b)

Figure 5.10: Simulated vacancy flux as a function of intermetallic compound thickness at a current density of 5.16×10^4 Amp/cm^2: (a) Cu_3Sn and (b) Cu_6Sn_5. (A negative sign indicates that the vacancy flux is moving in the direction from Sn solder to Cu under-bump metallization)

Figure 5.10 is of particular significance, because the stress-induced backflow that opposes the vacancy flux is also a function of the thickness. The stress-induced backflow can be described by Equation (1.6). This model does not account for the effect of stress-induced backflow due to a lack of information on the stress state of the solder joint. However, the stress-induced backflow is inversely proportional to the intermetallic compound thickness. Therefore, the variation of the stress-induced backflow can be estimated as the intermetallic compound thickens. Figure 5.11 shows the vacancy fluxes and the normalized stress-induced backflow in Cu_6Sn_5. The normalized backflow has been calculated using Equation (1.6), assuming the stress states at the boundaries of Cu_6Sn_5 are constant. The backflow occurs during electromigration to counter the vacancy flux and therefore is positive in sign.

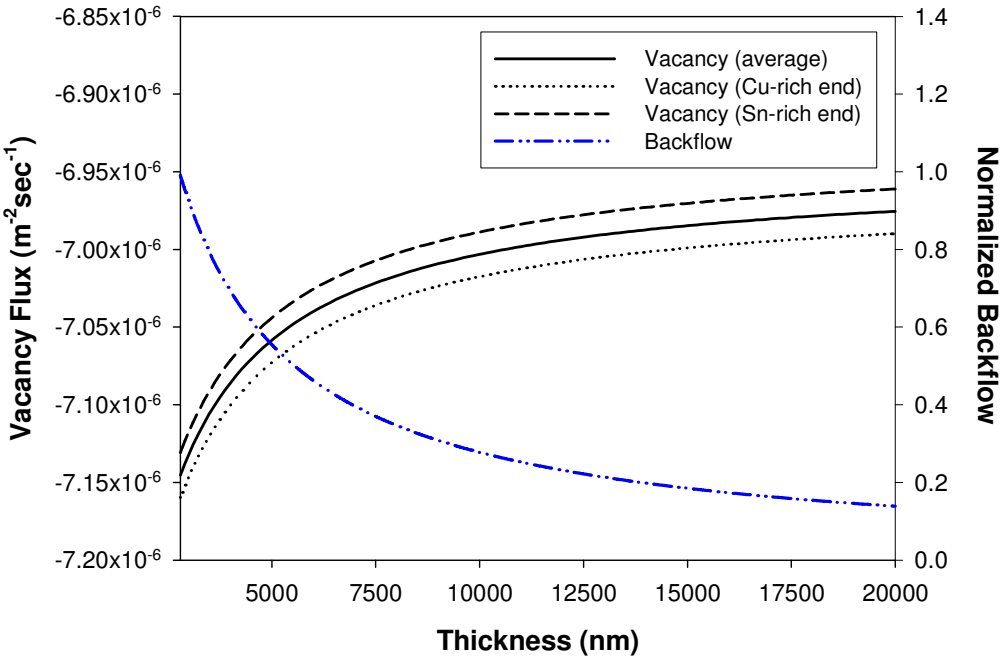


Figure 5.11: Vacancy flux in Cu_6Sn_5 with hypothetical stress-induced backflow

Stress-induced backflow is an important concept for interconnect technology, since the net vacancy transport can be counteracted by the stress buildup in a conductor below the critical length. With regard to electromigration in solder joints, the catastrophic void formation has been observed in Cu_6Sn_5 near the Cu_3Sn/Cu_6Sn_5 interface. This observation can be explained by the vacancy flux shown in Figure 5.11. When the vacancy flux is reduced from -7.15×10^{-6} $m^{-2}sec^{-1}$ to -6.97×10^{-6} $m^{-2}sec^{-1}$, a 2.5% reduction, the backflow is reduced by nearly 90%. This indicates that the vacancy flux remains nearly constant as Cu_6Sn_5 thickens; however, the backflow that counteracts the vacancy flux decreases significantly. This explains why the void formation occurs at Cu_6Sn_5 near the Cu_3Sn/Cu_6Sn_5 interface when the Cu_6Sn_5 thickens substantially. In addition, this result also suggests that suppression of Cu_6Sn_5 growth could play a critical role in reducing the void growth induced by current stressing. It will be very useful to be able to determine the critical length, that is, the Cu_6Sn_5 thickness at which the vacancy flux and backflow cancel each other out. In order to conduct such a study, analysis of the solder stress state due to intermetallic compound growth is required. This is a topic that will be studied in future work.

5.5 MODEL PREDICTIONS

The model has been used to make predictions about the effects of current density and Cu diffusivity in Sn solder on intermetallic compound kinetics. Studying the current density effect can assist in the design of accelerated electromigration testing to obtain critical results efficiently. Results from the study of the effect of Cu diffusivity in Sn solder can assist with the design of an optimal material to extend the lifetime of solder joints under electromigration.

5.5.1 Effect of Current Density

The growth of Cu_6Sn_5 under various current densities has been studied. Figure 5.12 shows the simulated Cu_6Sn_5 phase growth under various current stressing conditions for 300 hours. It shows that, above 1×10^4 Amp/cm^2, the simulated growth of Cu_6Sn_5 increases linearly with the current density. This indicates a linear effect on Cu_6Sn_5 growth enhancement by current stressing. However, the simulated growth is higher than the linear prediction for current stressing below 1×10^4 Amp/cm^2. This indicates that interdiffusion-induced growth becomes more significant at lower current densities.

Figure 5.13 shows the normalized Cu_6Sn_5 growth at three current stressing conditions: 5.16×10^4 Amp/cm^2 (100% of reference), 5.16×10^3 Amp/cm^2 (10% of reference), and 5.16×10^2 Amp/cm^2 (1% of reference). The growth in thickness is normalized to the growth from the 0th hour to the 300th hour of current stressing in order to compare the growth trends. At the high current density (5.16×10^4 Amp/cm^2), the growth trend is linear. At the low current density (5.16×10^3 Amp/cm^2 and 5.16×10^2 Amp/cm^2), Cu_6Sn_5 grows at a decaying rate indicating that the interdiffusion-induced growth is more pronounced when the current density is lower.

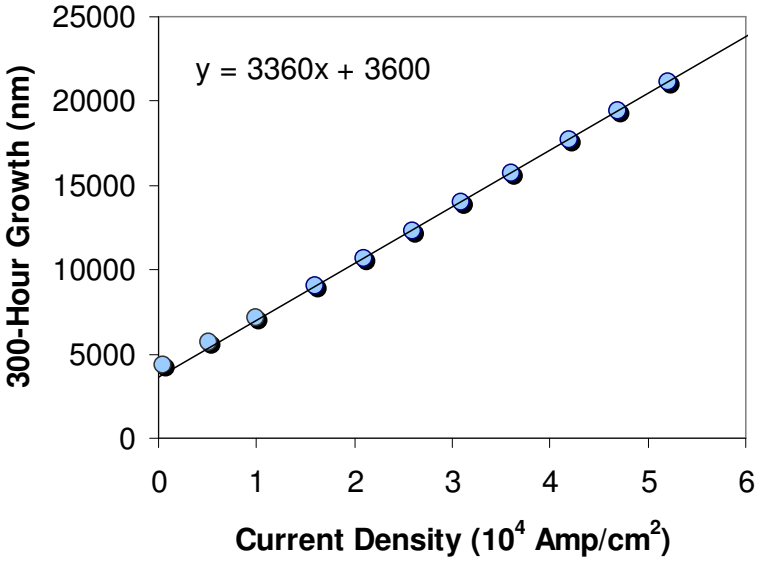


Figure 5.12: Simulated Cu_6Sn_5 compound growth under various current stressing conditions

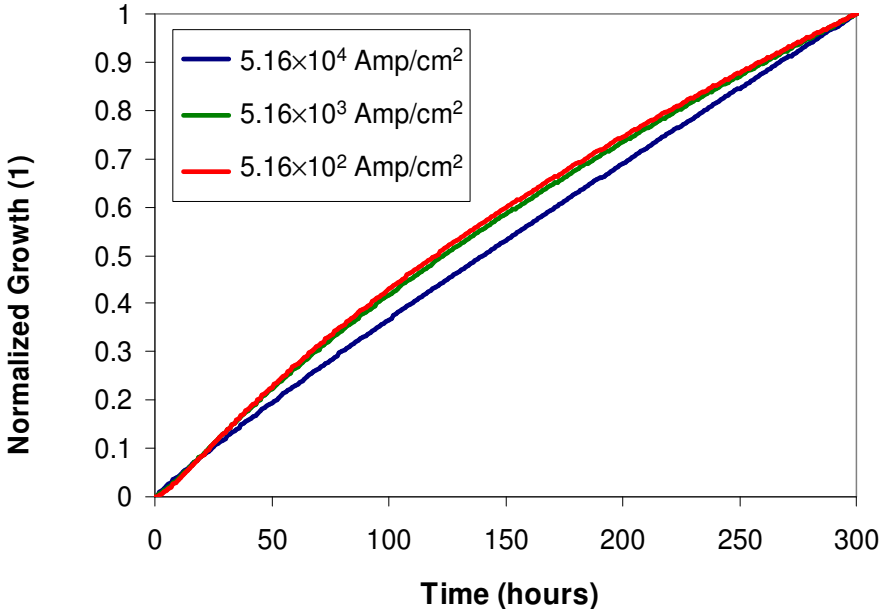


Figure 5.13: Simulated Cu_6Sn_5 growth under various current stressing conditions. (The data have been normalized to the data at 300 hours)

5.5.2 Effect of Cu Diffusivity in Sn Solder

It is widely known that the electromigration lifetime of Cu interconnects is controlled by Cu diffusion along the fast diffusion paths [5.5]. Therefore, the most rapid diffusion in the Cu-Sn system could play a significant role in controlling the electromigration lifetime of Pb-free solders on Cu under-bump metallization. As shown in Table 4.1, Cu diffusion in Sn solder is the most rapid in the Cu-Sn system and its diffusion coefficient is many orders of magnitude higher than those of the other phases. Anisotropic mobility of Cu atoms in Sn lattice was reported by Dyson *et al.*[5.6], who found that Cu diffusion along the *c* direction can be as much as 500 times more rapid than Cu diffusion perpendicular to the *c* direction. This anisotropic mobility could provide an opportunity for decreasing the Cu diffusion rate along the electron flux path by engineering the grain orientation of the Pb-free solder. Therefore, the model has also been used to study whether the intermetallic compound growth can be suppressed by reducing Cu diffusivity in Sn.

Figure 5.14 shows the simulated Cu_6Sn_5 intermetallic growths under 5.16×10^4 Amp/cm^2 current stressing when the Cu diffusivity in Sn solder is varied. The Cu diffusion coefficient used in the reference simulation was 1.5×10^{-11} m^2/sec, which is slightly lower than the literature value reported in Table 4.1. However, this value provided the best fit to the experimental data in the model validation based on simulated annealing, as described in Chapter 4. Two additional simulation runs have been conducted with identical parameters, with Cu diffusion coefficients of 1.5×10^{-12} m^2/sec, and 1.5×10^{-13} m^2/sec, respectively.

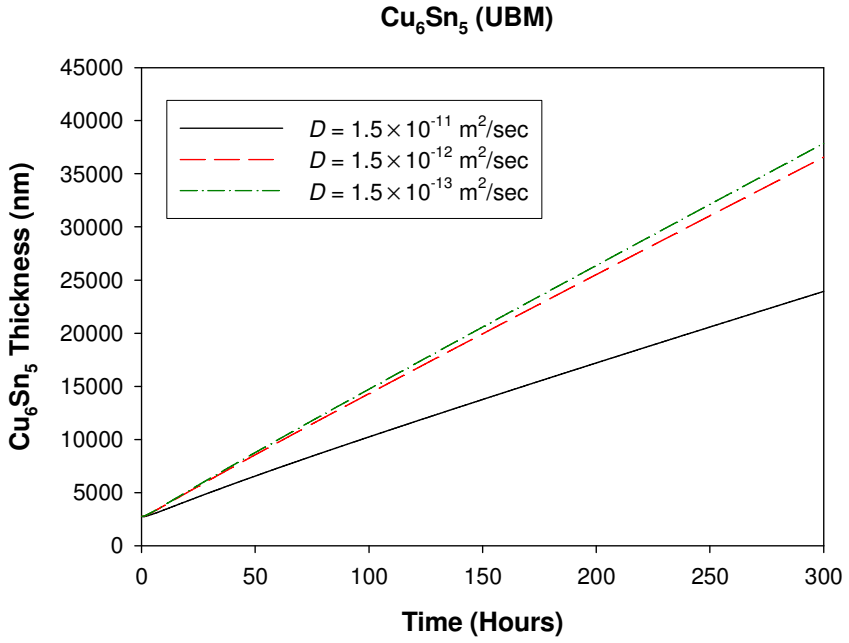


Figure 5.14: Simulated Cu_6Sn_5 growth at the under-bump metallization side obtained with various Cu diffusion coefficients in the Pb-free solder

As shown in Figure 5.14, decreasing the Cu diffusivity in Sn solder enhances the Cu_6Sn_5 growth, rather than reducing it. This is a surprising result since the objective of controlling Sn grain orientation has been to suppress intermetallic compound growth. The reason the model predicted enhanced Cu_6Sn_5 growth can be explained by the migration of the Cu_6Sn_5/Sn interface. When Cu diffusivity in Sn solder is high, the Cu atoms that are driven from Cu_6Sn_5 into Sn solder by electromigration are rapidly transported away. This increases the dissolution rate of Cu from Cu_6Sn_5 into the Sn phase and therefore Cu_6Sn_5 growth is reduced.

This prediction was made with the model that only took into account intermetallic compound growth at the under-bump metallization. Nevertheless, Figure 5.5 (a) shows that there is also Cu_6Sn_5 growth at the top surface metallurgy. Figure 5.5 (b) shows that

Cu_6Sn_5 at the under-bump metallization and at the top surface metallurgy can grow to connect with each other toward the end of the solder lifetime. One thick Cu_6Sn_5 phase is expected to have lower stress-induced backflow than two separate, but thinner, Cu_6Sn_5 phases. This could have an adverse effect on the solder lifetime by increasing the net vacancy flux toward the under-bump metallization side. Therefore, the Cu_6Sn_5 growth at top surface metallurgy has also been investigated as follows.

A Cu_6Sn_5 phase has been added to the model at the top surface metallurgy side, as shown in Figure 5.15. This additional Cu_6Sn_5 phase is not adjacent to the Cu-rich phase, such as Cu_3Sn. Therefore, its composition is assumed to be the lower limit of the Cu_6Sn_5 composition range. It is also assumed that Ni(P) serves as an effective diffusion barrier, that is, λ_5 is a fixed boundary and there is no mass transport across this boundary. This is a valid assumption, because the top surface metallurgy does not show any noticeable change, even when the solder joint has failed, as shown in Figure 2.4 (b).

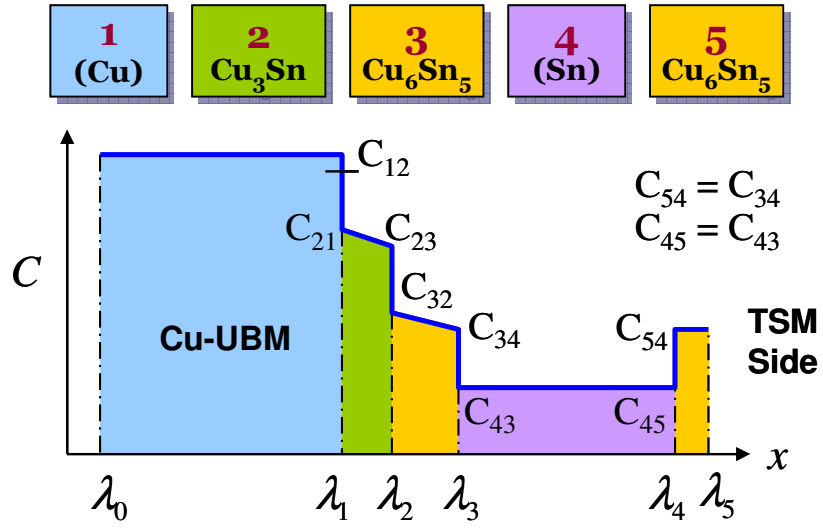
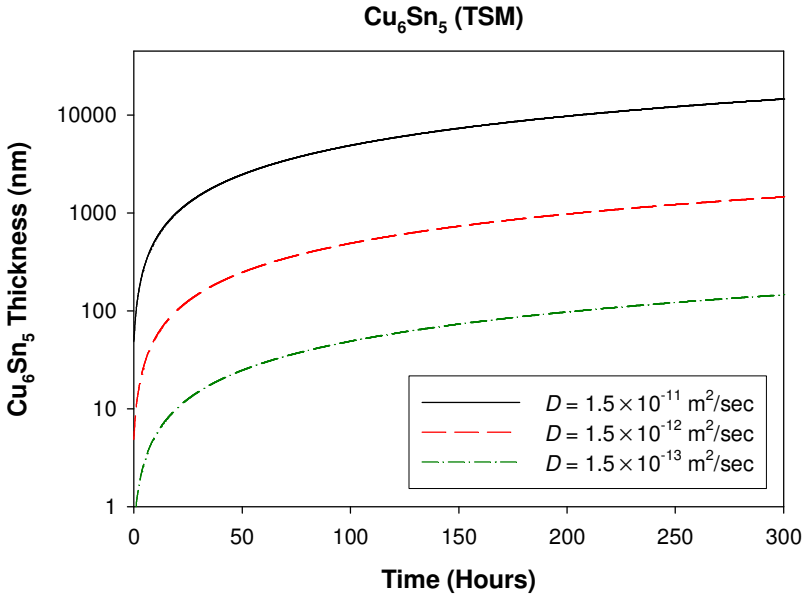


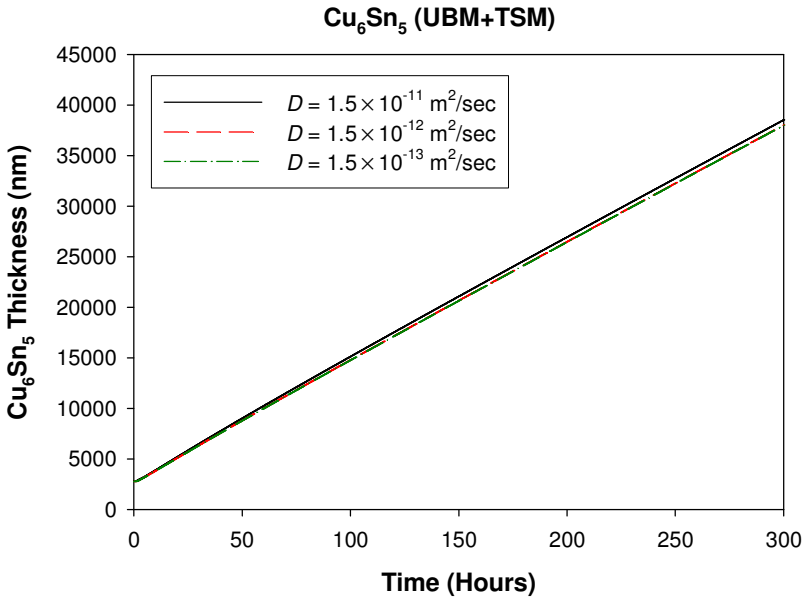
Figure 5.15: Layered structure which includes intermetallic compounds at both the under-bump metallization and the top surface metallurgy side

Using this expanded model, the effect of Cu diffusivity on the intermetallic compound growth under electromigration has been studied. Figure 5.16 (a) shows that Cu_6Sn_5 growth at the top surface metallurgy decreases with Cu diffusivity in Sn solder. Figure 5.16 (b) shows the overall Cu_6Sn_5 growth that includes Cu_6Sn_5 phases at both the under-bump metallization (Figure 5.14) and the top surface metallurgy (Figure 5.16 (a)). It shows that there is no significant difference in the overall Cu_6Sn_5 growth when the Cu diffusivity in Sn solder is varied for three orders of magnitude.

The results in Figure 5.14 and Figure 5.16 indicate that lower Cu diffusivity in Sn solder increases the Cu_6Sn_5 growth at the under-bump metallization, but decreases the Cu_6Sn_5 growth at the top surface metallurgy. In addition, the overall Cu_6Sn_5 phase growth at both sides of the solder joint is fairly independent of Cu diffusivity in Sn solder. This suggests that reducing Cu diffusivity in Sn solder will not suppress the overall Cu_6Sn_5 growth.



(a)



(b)

Figure 5.16: Simulated Cu_6Sn_5 growth obtained with various Cu diffusion coefficients in Pb-free solder: (a) growth at the top surface metallurgy, and (b) overall growth (at the under-bump metallization and the top surface metallurgy)

Chapter 6: Conclusions and Future Work

6.1 CONCLUSIONS

The model and simulation were established for the analysis of electromigration-enhanced intermetallic compound growth and void formation in an Sn-based Pb-free solder on Cu under-bump metallization. The analysis consisted of three components: an electromigration enhanced intermetallic compound kinetics model, a derivation of the diffusion and electromigration parameters, and a vacancy transport study. The kinetic model is a flux-driven model that takes into account Cu-Sn interdiffusion and the effects of current stressing. The complexity of the model with two intermetallic compounds necessitated the use of simulated annealing to efficiently estimate parameters such as diffusion coefficients and effective charge numbers for Cu and Sn atoms in the intermetallic compounds. The estimation of these parameters provided the foundation for the kinetic modeling that is critical to understanding diffusion behaviors in the intermetallic compounds, with or without current stressing.

The kinetic model has shown that both intermetallic compounds, Cu_3Sn and Cu_6Sn_5, follow a parabolic growth law during thermal aging. Under electromigration, the kinetic model indicated that Cu_6Sn_5 follow a linear growth law, but Cu_3Sn grows at a rate of decay faster than a $t^{1/2}$ law. The intermetallic compound growth rate has also been found to be linearly dependent on the current density when the current density is above 1×10^4 Amp/cm^2. Electromigration-induced void formation has been studied with the vacancy transport model. The results indicate that vacancies are being created in the intermetallic compounds and the direction of the net vacancy flux is toward the under-bump metallization, opposing the direction of the electron flux. The model has also shown that the net vacancy flux is greater in Cu_6Sn_5 than in Cu_3Sn, which causes the

vacancy concentration to increase substantially at the Cu_6Sn_5 side of the Cu_3Sn/Cu_6Sn_5 interface. This is the location where the accumulation of voids has been observed by others from their experiments. Finally, the effect of Cu diffusivity in Sn solder on the intermetallic compound growth has been studied. Cu has anisotropic diffusion coefficients in Sn solder which are dependent upon the Sn grain orientation. Therefore, it is possible to control Cu diffusivity in the direction of the electron flux by engineering the Sn solder grain orientation. The model predicted that Cu_6Sn_5 growth would increase at the under-bump metallization, but decrease at the top surface metallurgy. It also predicted that the overall Cu_6Sn_5 growth would still be comparable even if Cu diffusivity was reduced by 100 times.

6.2 FUTURE WORK

A two dimensional kinetic model, as shown in Figure 6.1, is an obvious and important extension based on the theoretical foundation established in this study. In the electromigration experiment, Cu_3Sn was found to form a conformal layer to Cu under-bump metallization, whereas the morphology of Cu_6Sn_5 followed the current path. The distinction in compound morphology cannot be explained with the one-dimensional model, but crucial insight can be gained with a two-dimensional kinetic model in this respect. In addition, the current crowding effect and diffusive flux divergence can be accounted for in compound growth kinetics and vacancy transport analysis.

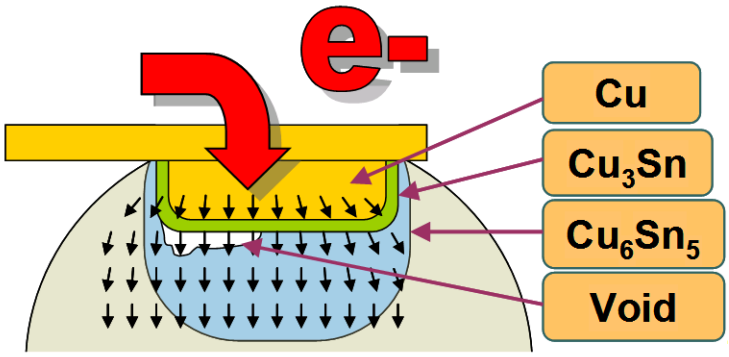


Figure 6.1: Two-dimensional kinetic model to address the current crowding effect and divergence of diffusive fluxes

Without formal derivation, the important equations are likely to take the following forms. For electromigration enhanced interdiffusion,

$$\frac{\partial C_i}{\partial t}=\tilde{D}_i \Delta C_i+\frac{\tilde{\phi}_i}{C_0} C_i (C_0-C_i)\nabla \bullet j \tag{6.1}$$

where $\Delta=\frac{\partial^2}{\partial x^2}+\frac{\partial^2}{\partial y^2}$, $\nabla=\hat{i}\frac{\partial}{\partial x}+\hat{j}\frac{\partial}{\partial y}$, and $\{\hat{i},\hat{j}\}$ is the standard basis in the two-dimensional space R^2.

For the kinetics of compound growth,

$$\begin{aligned}\vec{v}&=\vec{v}_{Chem}+\vec{v}_{EM}\\ &=\frac{1}{C_{\alpha\beta}-C_{\beta\alpha}}\left\{\left(\tilde{D}_\beta \nabla C_\beta-\tilde{D}_\alpha \nabla C_\alpha\right)+\vec{j}\left[C_{\beta\alpha}\left(C_0-C_{\beta\alpha}\right)\tilde{\phi}_\beta-C_{\alpha\beta}\left(C_0-C_{\alpha\beta}\right)\tilde{\phi}_\alpha\right]\right\}\end{aligned} \tag{6.2}$$

Finally, for the vacancy flux,

$$\vec{J}_{V,i} = \left(D_{Cu,i} - D_{Sn,i}\right)\nabla C_i - \left[C_i D_{Cu,i}\phi_{Cu,i} + \left(C_0 - C_i\right)D_{Sn,i}\phi_{Sn,i}\right]\vec{j} \tag{6.3}$$

However, it is by no means a simple undertaking to establish a model to solve Equations (6.1) to (6.3) and apply the model to a realistic solder joint structure. Significant breakthroughs will be needed in the numerical analyses to expand the current model to a two dimensional model.

MAJOR SECTION II

CU LOW-K DUAL DAMASCENE PROCESSING USING STEP AND FLASH IMPRINT LITHOGRAPHY

Chapter 7: Introduction

Step and Flash Imprint Lithography (S-FIL®) shows great promise as a cost effective solution to patterning sub 32 nm features and is capable of simultaneously patterning two levels of interconnect structures, which provides a high throughput and low cost Back End Of the Line (BEOL) process. Major Section II of this dissertation describes the integration of S-FIL into an industry standard Cu/low-k dual damascene process that is being practiced in SVTC Inc. in Austin TX (formerly Advanced Technology Development Facility, Inc.). The background information pertinent to this integrated study is given in this chapter. This includes the lithographic processes, the BEOL dual damascene integrated processing, and the pattern transferring reactive ion etch (RIE) process.

7.1 LITHOGRAPHIC PROCESSES IN MICROELECTRONICS FABRICATION

For the past four decades, the speed and density of computer processors has doubled approximately every 18 months, a trend known as the famous Moore's law. The realization of this trend was propelled by a constant advance in lithographic technology that allowed the industry to make ever smaller features using cost effective processes. This section gives a brief introduction to the photolithography process and the new lithographic technology that shows promise to extend miniaturization below 32 nm feature size.

7.1.1 Introduction to Photolithography

7.1.1.1 The Process

In microelectronic fabrication, the photolithographic process is used to transfer an image from a master pattern on a photomask onto a photoresist layer coated on the substrate. Figure 7.1 shows the main steps in photolithographic processing. A positive or a negative image can be transferred from the master pattern depending on the tone of the photoresist. The photomask consists of chromium patterns laid down on an amorphous quartz substrate. The chromium patterns constitute the opaque region on the transparent substrate. During the exposure step, ultra-violet (UV) radiation passes through the transparent regions of the photomask that were not covered by the chromium patterns, and is absorbed by a photosensitive polymer film, called a photoresist, on the surface of the substrate. UV radiation triggers photochemical reactions that alter the solubility of the exposed regions of the photoresist in a developing solvent. For a negative tone photoresist, the exposed areas become insoluble in the developer solvent. For a positive tone photoresist, the areas that are exposed to the UV light become soluble in the developer solvent. After the UV exposure step, the wafer is then subjected to the resist development step in which the highly solubility areas are selectively removed by dissolving into the developer solvent. After development, the image transferred from the master pattern on the mask is revealed.

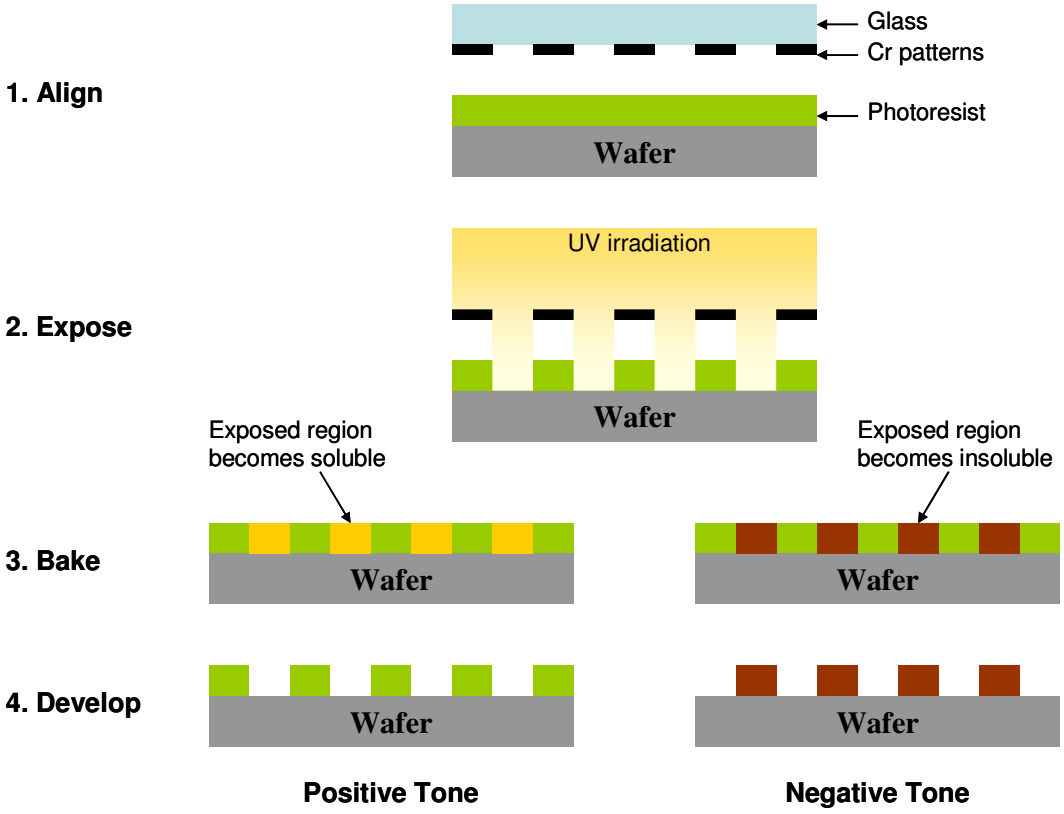


Figure 7.1: Photolithographic process using positive and negative tone photoresist

7.1.1.2 Resolution

The lithographic process is accomplished using reduction, projection lenses. The resolution R that determines the size of the smallest features that can be imaged on the wafer is governed by the famous Rayleigh equation.

$$R=\frac{k_1\lambda}{NA} \tag{7.1}$$

k_1 is a coefficient; λ is the exposing wavelength and NA is the numerical aperture of the lens. Therefore, resolution can be improved by reducing the wavelength

of the light source used during exposure, by increasing the numerical aperture of the projection lens or by reducing k_1.

The most significant advances in photolithography lie in the reduction of the exposure wavelength λ, from the g-line (436 nm) to the i-line (365 nm) of Hg discharge lamps, followed by deep UV KrF laser (248 nm) and then ArF laser (193 nm) radiation. The numerical aperture, *NA*, describes the amount of light that the projection lens can accept and focus on the photoresist. Therefore, high numerical aperture lenses enhance the resolution capability. k_1 is a process-related factor, which can be improved by the use of resolution enhancement techniques, such as phase shift masks, off-axis illumination, and optical proximity correction.

7.1.2 Next Generation Lithography (NGL)

A number of promising candidates for next-generation lithography technology have been identified by the International Technology Roadmap for Semiconductors (ITRS) [7.1]. They include Extreme Ultra-Violet lithography (EUVL), maskless lithography (ML2), nanoimprint lithography (NIL), and directed self-assembly. These technologies are considered the potential long term solution for the continuous quest for device scaling beyond 32 nm technology node. Figure 7.2 shows the potential solutions for imaging technologies for each generation.

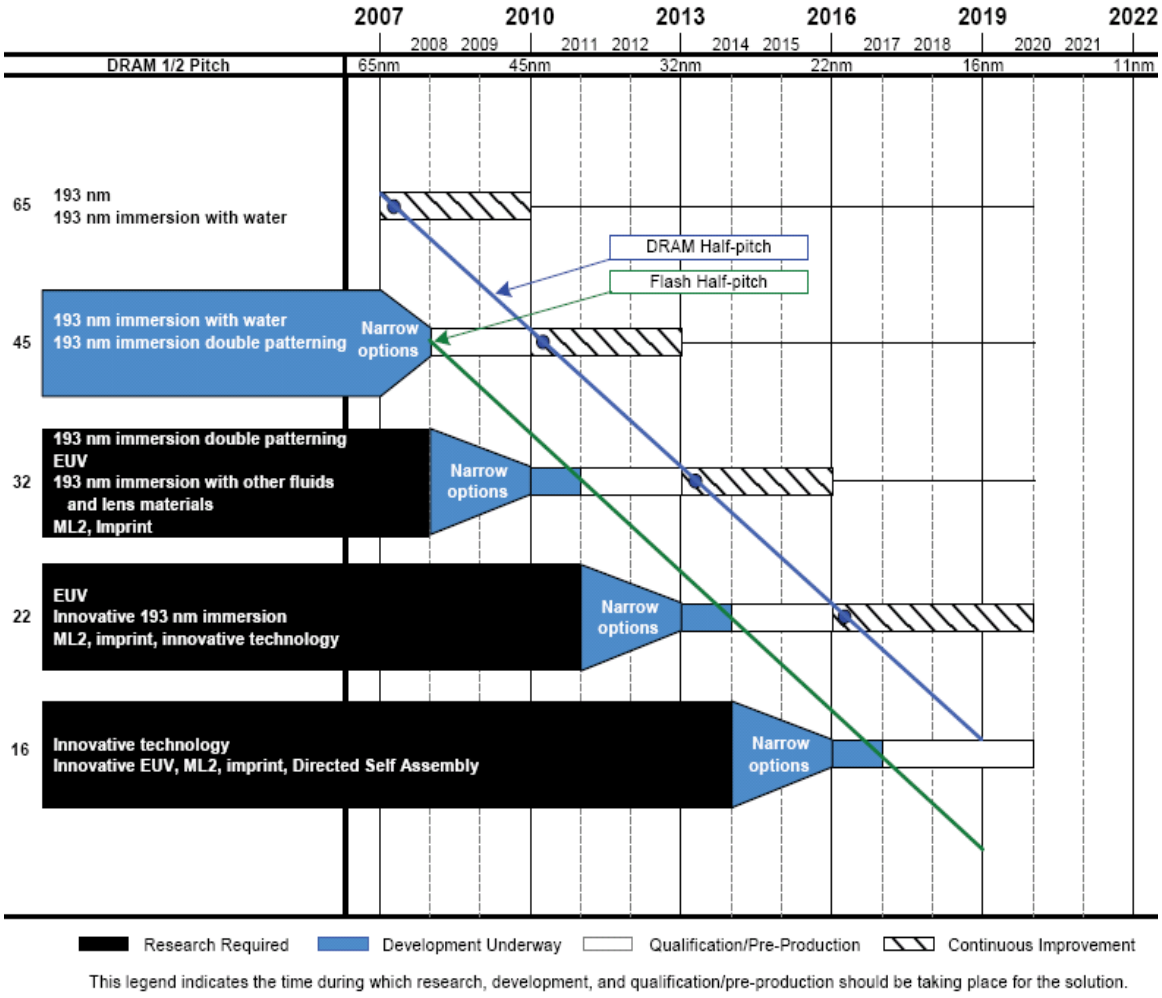


Figure 7.2: Potential solutions for exposure tools (Source: International Technology Roadmap for Semiconductors, Lithography, 2007 [7.1])

7.1.3 Step and Flash Imprint Lithography

Major barriers have emerged for sub 32 nm imaging by optical projection lithography, including soaring cost, poor photoresist performance, and delay in development of a high resolution Extreme UV (EUV) tool. Step and Flash Imprint Lithography (S-FIL) is considered to be one of the most promising candidates for next-generation lithography. It has the necessary high resolution with proven imaging capability of 22 nm on commercial tools and resists [7.2] and has very competitive cost of ownership (CoO) [7.3]. In contrast to electron or photon based lithographic approaches, S-FIL achieves pattern definition by photocuring a low viscosity liquid monomer formulation in a mold or template. The template can be made by the electron beam lithography. Therefore, S-FIL is capable of accomplishing imaging resolution beyond photolithographic limits. Images smaller than 10 nm have been replicated by this process [7.4]. Anything that can be etched into the template can be printed with high fidelity.

Figure 7.3 shows the process sequence of Step and Flash Imprint Lithography. A low-viscosity, photopolymerizable imprint liquid is first dispensed onto the substrate in a predetermined drop pattern. A quartz template with the patterned structures is then brought into contact with the imprint liquid at room temperature and under low imprint pressure, and the imprint liquid is allowed to fill the contours of the template. Once the filling is complete, ultra-violet radiation is used to polymerize the imprint liquid into a solid film, and finally the template is removed from the solidified imprint monomer. The hardened film then retains a negative replica of the patterns on the quartz template.

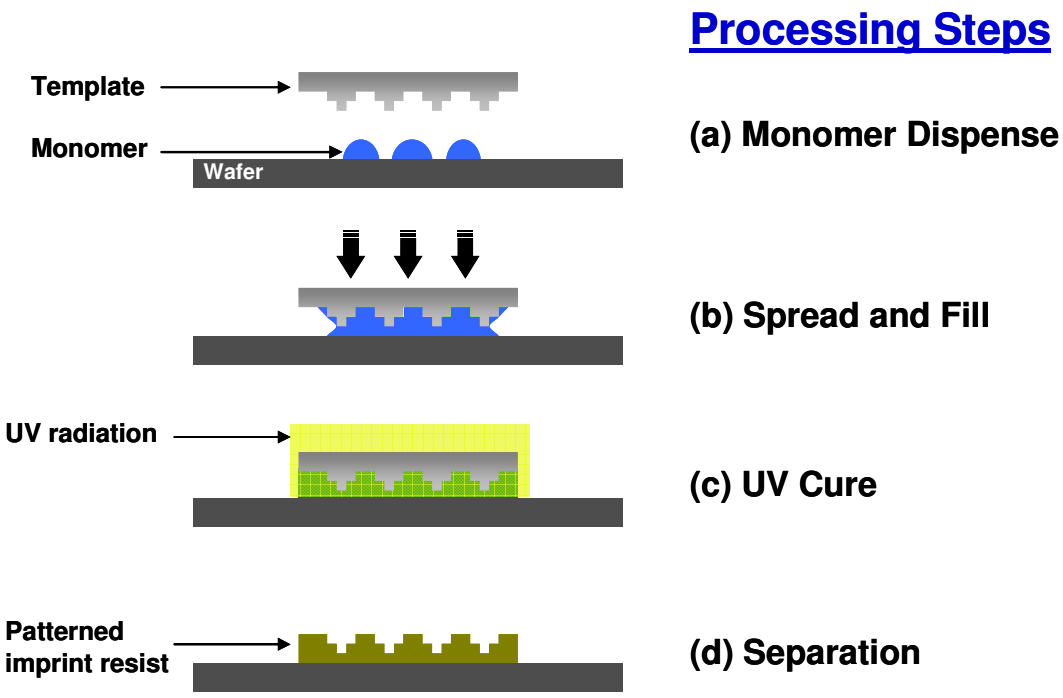


Figure 7.3: Step and Flash Imprint Lithography

7.2 Back End Of The Line (BEOL) Processing

The maximum clock speed of a micro processor is controlled by signal delay and clock skew. Signal delay is a combination of the gate delay and the interconnect delay. Figure 7.4 shows that the gate delay decreases but the interconnect delay rises drastically as devices are scaled down. Interconnect delay has been more serious than the gate delay in recent technology nodes and therefore become one of the main limiting factors in the performance of the advanced integrated circuits. The optimization of the BEOL technology requires extensive research and development in layout and structure design schemes, improvement of materials, and fabrication processes.

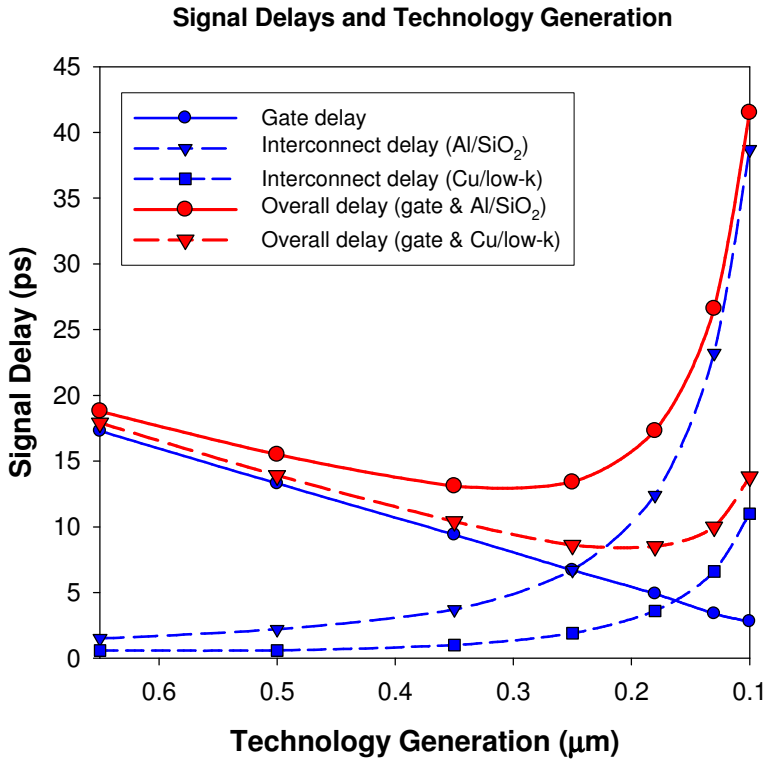


Figure 7.4: Delay as a function of feature size (Source: M. T. Bohr in Ref [7.5] and S. C. Sun in Ref [7.6]; this graph was replotted by the author)

7.2.1 Materials

The interconnect delay can be characterized by the product of *R*, the interconnect resistance, and *C*, the capacitance of the inter-level dielectrics (ILD). To reduce the resistance of the interconnects, Copper (Cu) has been used in advanced interconnect technology to replace aluminum (Al) for its superior conductivity [7.7,7.8]. To reduce the capacitance of the ILD, low dielectric constant (low-k) has been employed to replace SiO_2 [7.9]. Figure 7.4 indicates the significant reduction in *RC* delay with the incorporation of Cu and low-k dielectrics compared to the conventional interconnect technology that uses Al and SiO_2 [7.5,7.10].

7.2.2 Cu/low-k Dual Damascene Processing

7.2.2.1 Standard Process

The state of the art Back End Of the Line (BEOL) process employs Cu interconnects and a low dielectric constant (low k) inter-level dielectric (ILD). These Cu interconnects are made with the dual damascene process and comprise via and line structures. Vias are interconnects that transmit signals between planes of wiring; lines are wires that distribute signals within the plane of each interconnect level. The line structures are also referred to as "trenches" because they are subtractively etched into the dielectrics. Due to lack of a volatile Cu etch product, the subtractive etching schemes that were used to pattern Al interconnects are not applicable for Cu technology [7.8]. Therefore, dual damascene processing was developed. In this process, the desired patterns are etched into the dielectrics before subsequently filling them with Cu to produce the lines and the vias. Because Cu atoms can rapidly diffuse into low-k dielectrics, diffusion barriers are needed to prevent Cu diffusion and provide adhesion to both Cu and the low-k material [7.11,7.12]. The common diffusion barriers used for the sidewalls and bottoms of the conductors are tantalum (Ta) or tantalum nitride (TaN). The diffusion barriers used between two layers are usually silicon nitride (SiN) or silicon carbide (SiC) [7.11,7.12].

The "via first" and the "trench first" processes have both been developed for dual damascene processing. [7.8]. The via patterns are etched first into the dielectrics in the via first process whereas the trenches are patterned first in the trench first process. The via first approach is more widely practiced in the industry because the trench first

approach requires imaging of the small vias over the topography of the existing line patterns in the dielectrics and this was found to be very difficult [7.8].

Figure 7.5 shows the conventional via first dual damascene process flow using photolithography. The process requires two lithography steps, two etching steps, and several additional processing steps, such as resist stripping, etc. Cu/low-k technology has provided significant improvement in the interconnect performance and reliability. However, it also introduced new integration and reliability challenges and producing these structures requires a very large number of process steps.

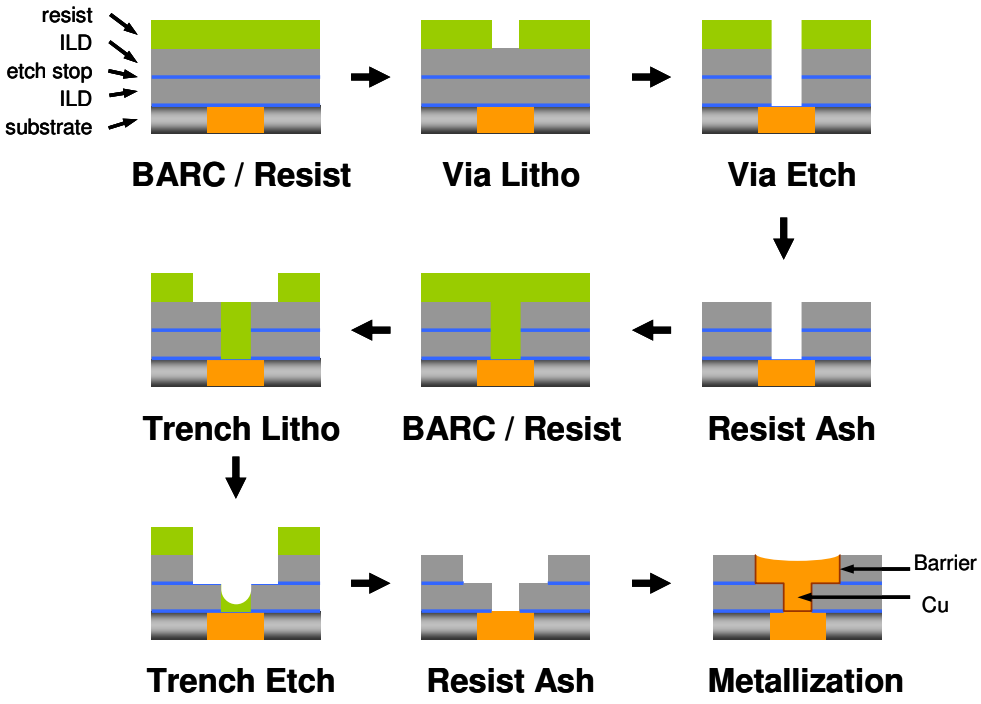


Figure 7.5: Standard dual damascene processing sequence (Source: G. M Schmid *et al.* in Ref [7.13]; this graph was replotted by the author)

7.2.2.2 Dual Damascene Processing Using Multilevel S-FIL

The conventional dual damascene processing requires separate lithography and etching steps to pattern the vias and the lines prior to the metallization and chemical mechanical polishing (CMP) steps that complete each of the wiring levels. The process has become increasingly complex and costly because as many as ten or more wiring levels are needed in advanced chip designs.

It was proposed by the Willson Research Group that S-FIL in conjunction with a multilevel template might provide a new approach to dual damascene processing, which could significantly reduce the number of steps required to build the interconnect structures [7.13] and thereby lower the wafer processing cost [7.3,7.14]. Schmid [7.13] showed that one imprint lithography step can produce the same resist pattern as two photolithography steps through use of a multilevel template on which both the via and the line features are incorporated. The purpose of the work described in this thesis was to determine whether this new resist processing technique can provide a high yield and low cost solution to the fabrication of BEOL interconnects by integration into an industry standard process in conjunction with electrical testing.

Figure 7.6 shows the multilevel S-FIL dual damascene process flow. Multilevel S-FIL allows both the via and the line patterns to be combined onto the same master template and imaged onto the wafer in one lithographic step. The resulting pattern containing both vias and lines can, in principle, be subsequently transferred into the ILD in one etch step. Because the via-to-line overlay was done in template fabrication, these two levels are effectively self-aligned during wafer processing. The greatly simplified flow removes at least three of the most expensive processing steps on each interconnect

level and therefore has the potential of providing tremendous cost saving. Industry estimates of 20 to 50% saving on wafer cost have been published [7.3,7.14].

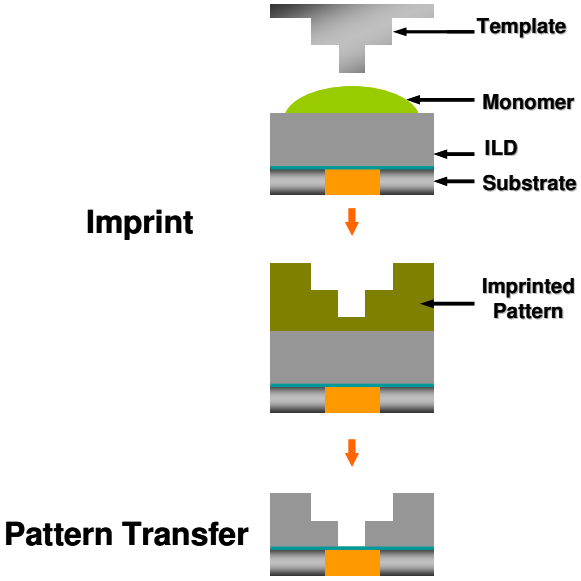


Figure 7.6: Dual damascene processing using multilevel Step and Flash Imprint Lithography (Source: G. M Schmid *et al*. in Ref [7.13]; this graph was replotted by the author)

7.3 REACTIVE ION ETCHING OF INTER-LEVEL DIELECTRICS

Low-pressure plasma discharges are widely used for etching microscopic features in integrated circuits. Electrons are accelerated by Radio Frequency (RF) or microwave electric fields and collide inelastically with precursor molecules in the gas phase to produce ions, atoms, and radicals. A complex mixture of reactive species is produced in this manner. During the etching process, neutral and ionic reactive species strike the surfaces that are in contact with them to form products that are volatile.

As described in Section 7.2, the etching chemistry needed for dual damascene processing is one which etches the dielectric materials, SiO_2 or the low-k materials.

Halocarbon gas mixtures that produce fluorine atoms and fluorocarbon compounds are widely used in the reactive ion etching (RIE) of SiO_2. Fluorine atoms react spontaneously with SiO_2 to form volatile products [7.15]. However, etching chemistry based predominantly on fluorine radicals is chemically aggressive and does not produce the vertical sidewalls required for high density patterning. Therefore, commercial RIE tools for dielectric etching usually employ fluorocarbon chemistries. The most widely used etching gases include CF_4, C_2F_6, C_3F_8, *cyclo*-C_4F_8, etc. The plasma etchants and their reactions were reviewed by Flamm and Donnely [7.16].

In contrast to fluorine atoms, studies showed that etching of SiO_2 with fluorocarbon radicals is not spontaneous and only occurs when the surface is subject to simultaneous ion bombardment [7.17,7.18]. Etching reactions take place in the ion bombarded SiO_2 surface and produce volatile byproducts. Without sufficient ionic interaction with the surface, a polymeric fluorocarbon film forms and grows on the SiO_2 surface. The transition from etching to deposition in a fluorocarbon plasma with respect to ion energy flux was observed by Oehrlein [7.19] and an example is shown in Figure 7.7 [7.19,7.20]. In regime (a), the ion bombardment energy is low, and a fluorocarbon layer is deposited on the SiO_2 surface instead of SiO_2 etching. In regime (b), the ion bombardment energy is high enough for SiO_2 etching to occur, however, there is still a fluorocarbon layer forming concurrently on the SiO_2 surface. This fluorocarbon layer suppresses the SiO_2 etching rate, but the suppression effect decreases as the ion bombardment energy increases. In regime (c), the ion bombardment energy is high. Above a certain energy, the SiO_2 etch rate becomes independent of the ionic bombardment energy and is only controlled by the chemical etch rates. This result was reported by Oehrlein [7.19]. The etching chemistry that is able to produce simultaneous polymer deposition is commonly referred to as a “polymerizing” chemistry in the plasma

etching terminology. The ability to control whether etching or deposition is to occur locally is critical to the anisotropic etching that produces vertical sidewalls in microscopic features.

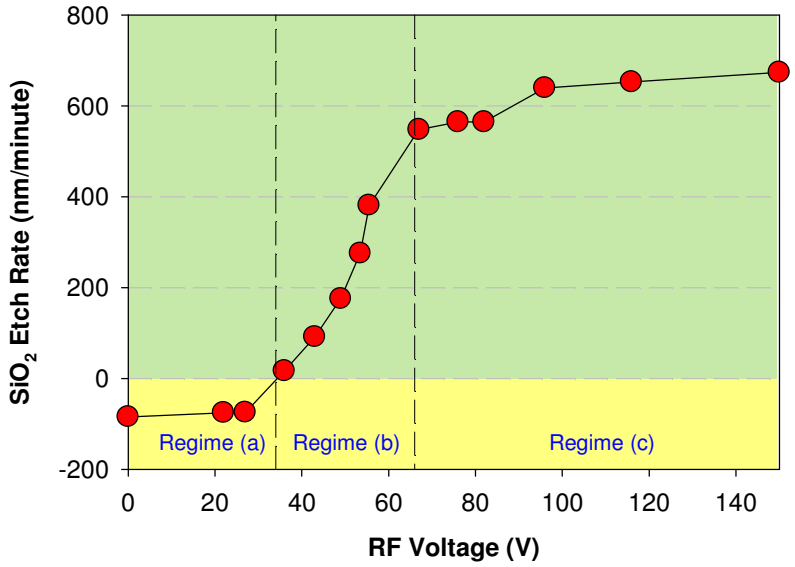


Figure 7.7: An example of a deposition-to-etching transition in CF_4 chemistry caused by increasing ionic energy flux at a surface: (a) fluorocarbon deposition, (b) fluorocarbon suppression, and (c) oxide etching regimes; yellow areas indicate fluorocarbon deposition and green areas indicate SiO_2 etching (Source: G. S. Oehrlein, *et al*. in Ref [7.19] and also reviewed by G. S. Oehrlein and K. Yukinori in Ref [7.20]; this graph was replotted by the author)

Control of lateral etching of the microscopic feature requires the formation of passivation layers on the vertical walls and takes advantage of the etch-to-deposition transition described above. Figure 7.8 shows the etching and deposition events that occur simultaneously in a microscopic structure. The red arrows show the line-of-sight trajectory of the ionic species. Blue arrows show the diffusion of the neutral radicals which facilitate etching or deposition depending on the surface upon which the reactions

take place. The green arrows indicate the resputtered surface species, which deposit on the surface.

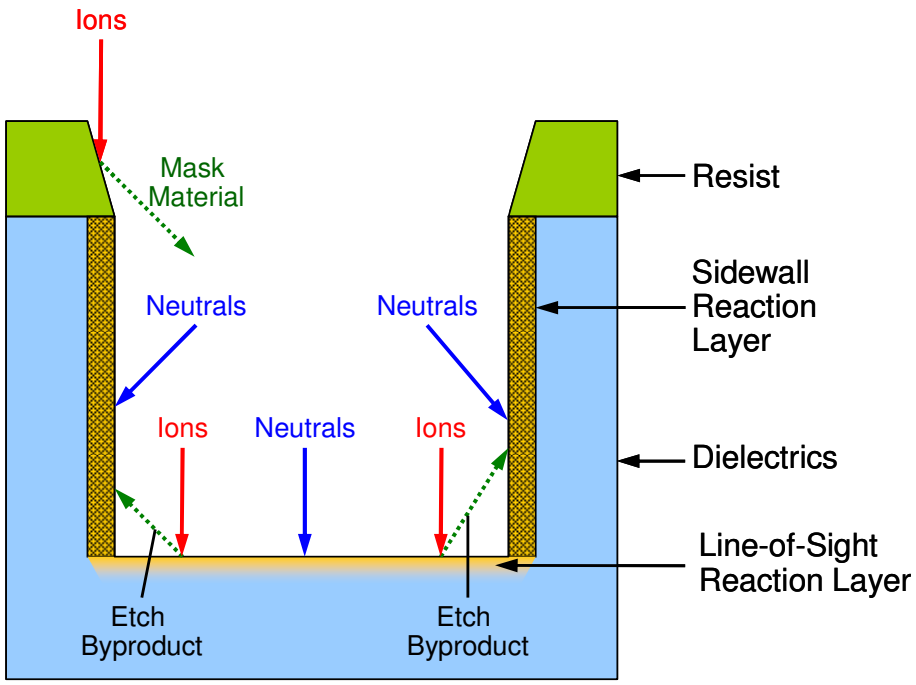


Figure 7.8: Critical chemical and physical events during reactive ion etching of SiO_2 or silica based dielectrics in fluorocarbon plasmas (Source: G. S. Oehrlein and Y. Kurogi in Ref [7.20]; this diagram was replotted by the author)

As shown in Figure 7.8, the surface chemistry is significantly altered by the ion bombardment. At the bottom of the microstructure, the surface is subjected to the ion bombardment directed by the potential difference between the plasma and the substrate. Etching can take place at the bottom of the microstructure because the reactions operate in regimes (b) or (c) as shown in Figure 7.7. At the sidewalls, the surface is subjected to significantly reduced ion bombardment energy. Therefore, a fluorocarbon layer is deposited and little or no lateral etching takes place because the reactions at the sidewall

operate in regime (a). This difference in surface reactions results in the etching process that produces vertical sidewalls.

7.4 OBJECTIVE AND APPROACH

The goal of the work described in this thesis was the first experimental demonstration of the utility of S-FIL patterning technology for production of interconnect-circuits on microelectronic devices. This work required bringing together new template structures, new materials, new test vehicle designs, new etch processes and new metrology techniques. Our approach was to integrate multilevel S-FIL into an industry standard Cu/low-k dual damascene process that is being practiced in SVTC in Austin, TX. BEOL test structures were incorporated into the pattern design and the template and mask required were fabricated to specification by a commercial mask house. The yield of this test vehicle was investigated to evaluate the effectiveness of the new integration scheme.

The design of the test vehicle is described in Chapter 8, and the multilevel S-FIL process is described in Chapter 9. The pattern transferring reactive ion etching (RIE) process, the most critical step in the integration, was extensively explored in this study. An *in-situ*, multistep etch process for pattern transfer was developed and is described in Chapter 10 and 11. This new approach gives excellent pattern structures in two industry standard Chemical Vapor Deposited (CVD) low-k dielectrics. Chapter 12 describes the correlation between process variation and yield together with a discussion of the failure mechanisms that are characteristic of the multilevel S-FIL process.

The author conducted the experiments required to optimize the process to achieve imprint uniformity in collaboration with Dr. Frank Palmieri, Dr. Kang Luo, and Kane Jen. All etch experiments were designed and conducted by the author on wafers

imprinted by Dr. Frank Palmieri, Kane Jen or Dr. Kang Luo. The metallization processes were designed by the author, and conducted by or with the assistance of the engineers of SVTC. The electrical testing was programmed by Bruce Wilks of SVTC and analyzed by the author. The new via chain design was proposed by the author.

The key contributions of this work:

1. An *in-situ* multi-step etch scheme was developed that provides a faithful pattern transfer of the multilevel structures, which would be difficult to achieve with the conventional single-step etch process. This discovery is discussed in Chapter 10 and 11.
2. Multi-level Step and Flash Imprint Lithography was demonstrated for the first time to be a viable candidate for the Cu/low-k Back End Of the Line processing through the study of the yield of a dual damascene test vehicle. Imprint-specific issues were identified that are pertinent to the process, test methods, and yield.

Chapter 8: Dual Damascene Test Vehicle and Multilevel S-FIL

8.1 INTRODUCTION

Successful integration of multilevel S-FIL into the dual damascene process requires imprint templates with multilevel interconnect features, an imprint tool with overlay capability, and BEOL processing and qualification capability. Details regarding these critical ingredients are given in this chapter.

8.2 DUAL DAMASCENE TEST VEHICLE

8.2.1 Test Structures

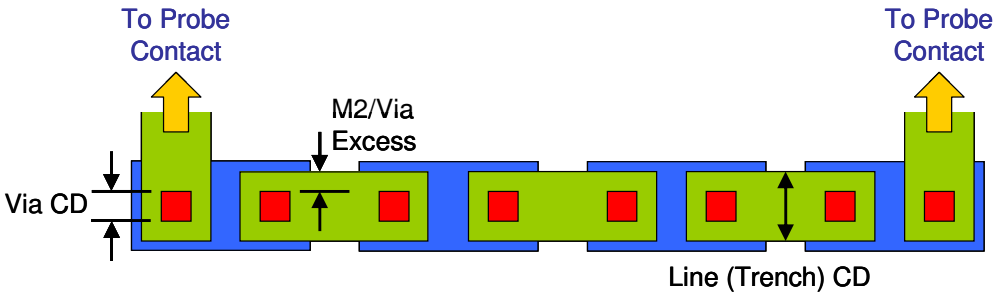
In order to investigate the dual damascene process using S-FIL, a host of electrical test structures of various sizes were incorporated onto the template. These test structures include via chains, Kelvin arrays (single vias), various line structures and interdigitated serpentines.

8.2.1.1 Kelvin Vias and Via Chains

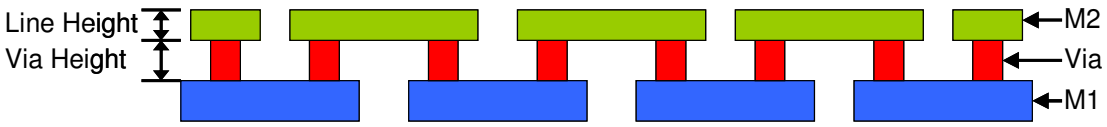
Kelvin vias and via chains are the most important test structures because they indicate whether the connection between the Metal 1 and Metal 2 (M1 and M2) levels are properly connected to close the circuits. A Kelvin via structure contains only one via whereas a via chain structure contains many. In the via chain structures, the vias are connected in a series, or chain, as shown in Figure 8.1. The critical dimension (CD), or width, of vias or lines is usually limited by the resolution of the lithographic technology. Various M2/via excesses, as shown in Figure 8.1 (a), were designed into the test vehicle to accommodate the uncertain alignment capability of template fabrication. No such

template had ever been made before. Incorporation of via chains with large M2/via excesses insures that some via chains on the template are still valid even if some small misalignment occurred during template fabrication. Incorporation of via chains with small M2/via excesses allows investigation of the features with critical characteristics similar to actual microelectronic devices.

Yield statistics can be deduced efficiently with via chain test structures. This is because open circuit failure of a single via in the chain causes the entire chain to fail and this failure can be detected by resistance measurements. The template used in this work contains via sizes ranging from 120 nm to 2 µm and chain lengths from 10 contacts to 1000 contacts long. Additional long chains up to 150,000 contacts were also incorporated for via sizes 0.5, 0.75, 1, and 2 µm. The characteristics of the via chains are listed in Table 8.1 and Table 8.2.



(a)



(b)

Figure 8.1: Dual damascene via chain: (a) top-down, and (b) cross sectional diagram

Table 8.1: Via chains of critical via CD

M2-via excess	700 nm	200 nm	0 nm
Via CD (nm)	120, 130, 140, 150, 200, 250, 350, 500, 750	120, 130, 140, 150, 200, 250, 350, 500, 750	200, 250, 350, 500, 750
Chain Size (# of contacts)	10, 100, 1000	10, 100, 1000	10, 100, 1000

Table 8.2: Via chains of critical chain length

Via CD	500 nm, 750 nm, 1 μm, 2μm
Chain Size (# of contacts)	150,000 contacts. (Taps at 1,000; 10,000; 24,000; 50,000; 74,000; 100,000; 124,000; and 150,000)

8.2.1.2 Dense Lines

Various line structures were also included in the test vehicle and they are shown in Figure 8.2. These line structures are also electrically testable. Isolated lines and dense lines features are self-explanatory. Serpentines are very long lines, which can be accommodated in a relatively small footprint. Comb structures can detect bridging between adjacent lines and can be used to measure the ILD capacitance. Serp/Comb structures combine serpentines and combs and therefore have the advantage of both.

The line and spacing in the template design include the following: 125 nm / 175 nm, 150 nm / 200 nm, 175 nm / 225 nm, 200 nm / 250 nm, 225 nm / 275 nm, 250 nm / 300 nm, 300 nm / 350 nm.

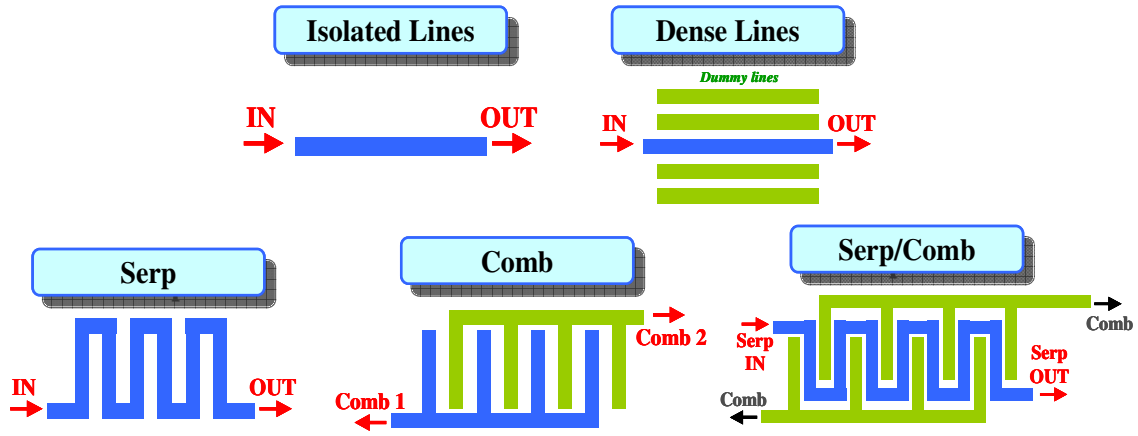


Figure 8.2: Various line structures

8.2.2 Film Stack and Metal 1 (M1) Processing

Two inter-level dielectrics (ILD) materials were used in the etch experiments, CORAL® by Novellus, Inc., San Jose CA and Black Diamond® by Applied Materials, Inc., Santa Clara CA. Both are low dielectric constant ILD materials deposited by plasma-enhanced chemical vapor deposition (PECVD). Only CORAL® was used in the electrical yield experiment due to the in-house deposition capability of this material at SVTC. Nitrogen doped silicon carbide (SiCN) was used as the cap layer, which mainly serves two purposes: a) preventing Metal 1 Cu from oxidizing prior to Metal 2 processing and b) as a diffusion barrier between Metal 1 Cu and Metal 2 ILD. All ILD and cap layer materials used in this paper are industry accepted materials for nonporous, low k BEOL products. The dielectric material used in Metal 1 level was standard CVD SiO_2.

Multilevel S-FIL was used for via and Metal 2 lithography and 248 nm photolithography was used for Metal 1 patterning. Figure 8.3 indicates the objective product of this test vehicle from M1, via, to M2 levels. It also shows a diagram of a 4-contact via chain module with probe pads connected to the terminals of the chain for electrical testing.

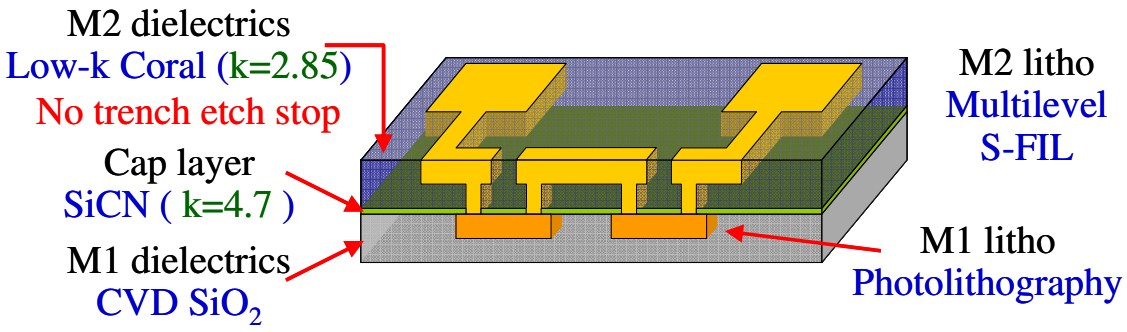


Figure 8.3: Diagram of the film stack and a via chain test structure.

8.2.3 Multilevel Template

The template used in this study incorporates both the via and the line features of the dual damascene BEOL test vehicle. The active area on the template is 25 mm by 25 mm. It includes four quadrants and each quadrant contains top and bottom halves, as shown in Figure 8.4. Pattern designs are identical for the top and bottom halves and for all quadrants. This means that all features have 8 duplicates on the template. The unused area between test structures is filled with dummy features to maintain a constant pattern density for improved chemical mechanical polishing (CMP) uniformity. The multilevel templates designed for this project were purchased from Toppan Photomasks, Inc., Round Rock TX [8.1].

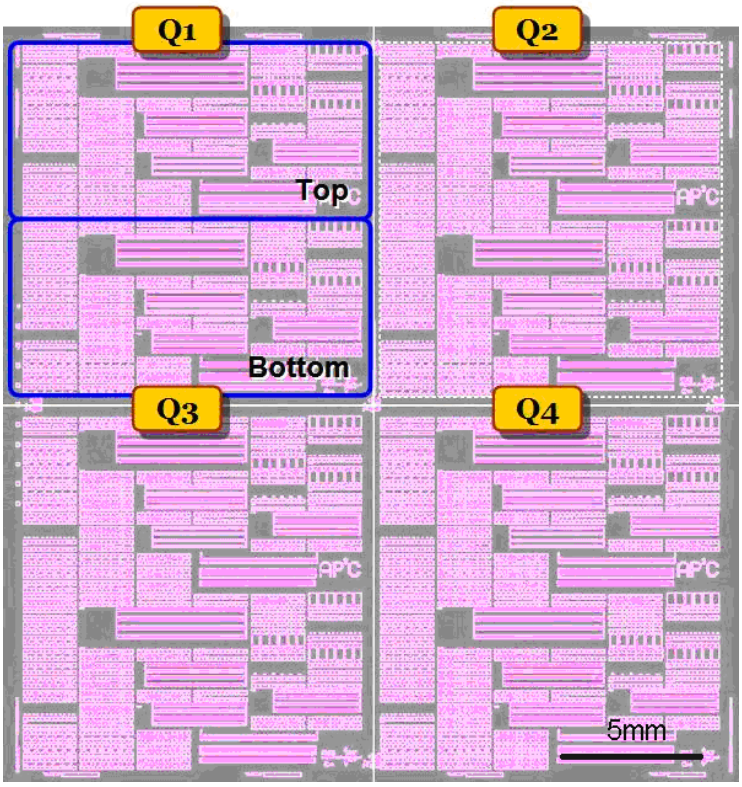
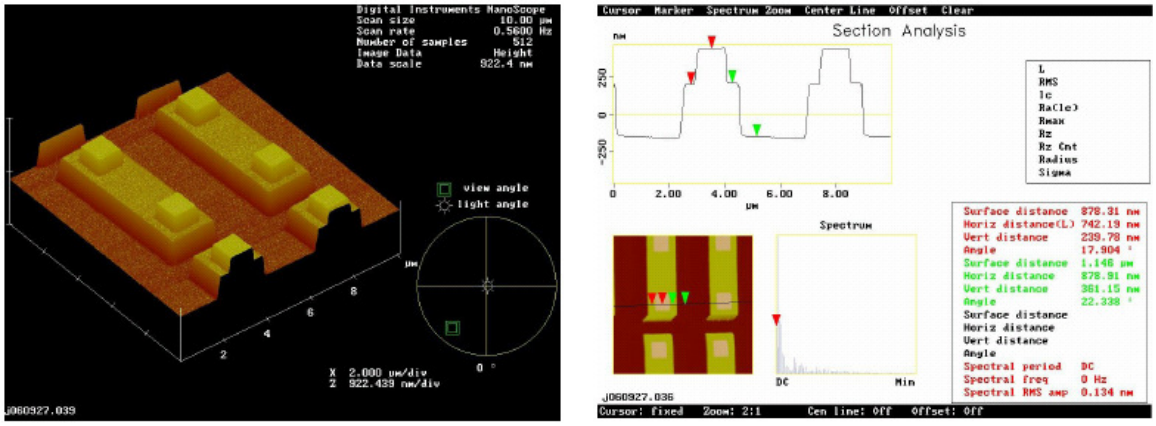


Figure 8.4: Template floor plan

Figure 8.5 shows direct inspection of the multilevel template by Atomic Force Microscope (AFM), which clearly indicates the incorporation of both the vias and lines of the dual damascene feature. Table 8.3 shows the feature height on the multilevel template obtained by the AFM measurement. Figure 8.6 and Figure 8.7 show the scanning electron microscope (SEM) measurement of various via structures and dense lines structures on the template. These characterization results of the multilevel template were provided by Toppan Photomasks. While this template was not perfect, it is fully acceptable and demonstrates the ability of the existing photomask manufacturing community to produce such parts using their standard processes.



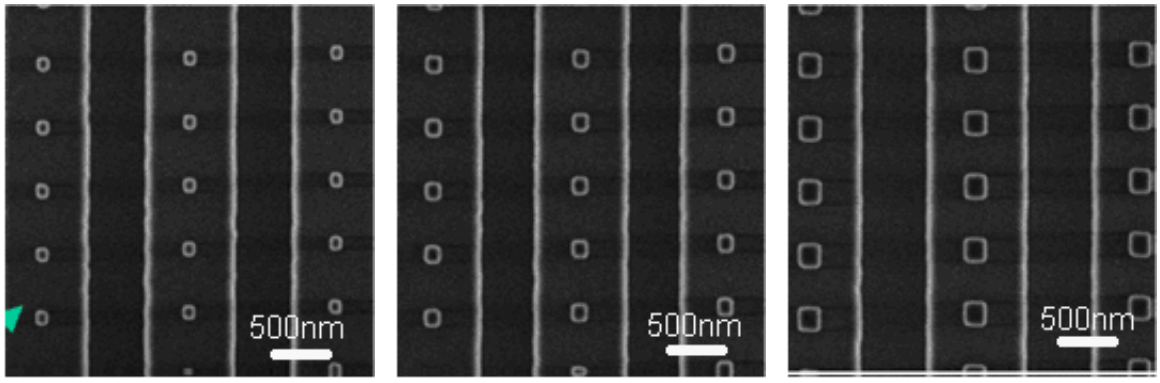
(a) (b)

(Source: Toppan Photomasks, Inc.)

Figure 8.5: Investigation of a 1 µm via chain on the multilevel template using atomic force microscopy (AFM): (a) surface profile, and (b) feature height measurement

Table 8.3: Measured feature height of the multilevel template (Source: Toppan Photomasks, Inc.)

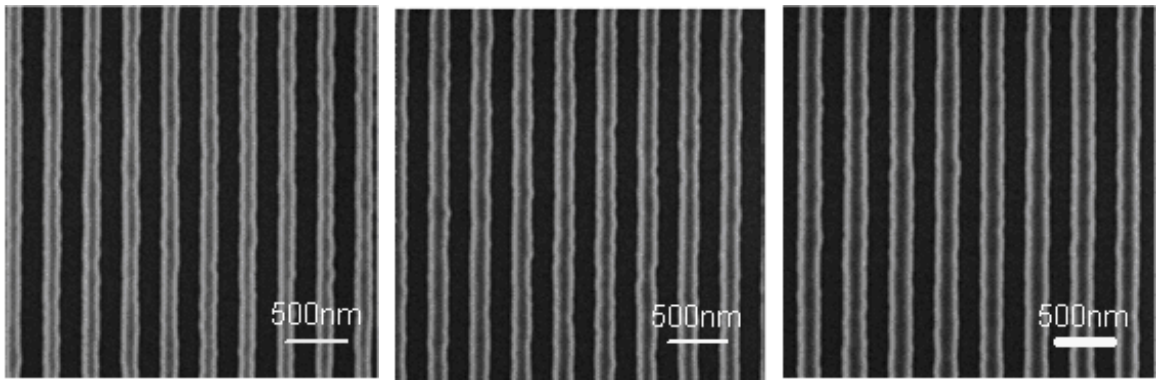
Level	Measured Height
Via	240 nm (measured with residual Cr)
Metal 2	362 nm



(a) (b) (c)

(Source: Toppan Photomasks, Inc.)

Figure 8.6: Investigation of various via structures using SEM: (a) 120 nm, (b) 150 nm, and (c) 200 nm vias



(a) (b) (c)

(Source: Toppan Photomasks, Inc.)

Figure 8.7: Investigation of various dense line structures using SEM: (a) 125 nm /175 nm, (b) 150 nm / 175 nm, (c) 175 nm / 175 nm (line width/spacing)

8.3 MULTILEVEL STEP AND FLASH IMPRINT LITHOGRAPHY

In this study, the imprinting was accomplished with Imprio 55 and Imprio 100 tools from Molecular Imprints, Inc., Austin TX. The etch experiment wafers were imprinted with the Imprio 55 in Professor C. Grant Willson's laboratory in the Chemical Engineering Department, the University of Texas at Austin, and with Imprio 100 in the Microelectronics Research Center, the University of Texas at Austin. The wafers used in electrical yield experiments were imprinted with Imprio 100 in Molecular Imprints, Inc. Figure 8.8 shows the Imprio 100 S-FIL system.

In order to provide conductivity of the via chains for electrical testing, the Metal 2 patterns need to be properly aligned to Metal 1 patterns. Therefore, both the multilevel template and the Metal 1 photomask patterns include Imprio 100 alignment patterns. Imprio 100 systems are capable of performing automatic alignment with registration to 500 nm or better. On the Imprio 55 system, alignment was performed manually.

(Source: Molecular Imprints, Inc.)

Figure 8.8: The Imprio 100 S-FIL system from Molecular Imprints Inc.

Chapter 9: Multilevel S-FIL Process Optimization

9.1 INTRODUCTION

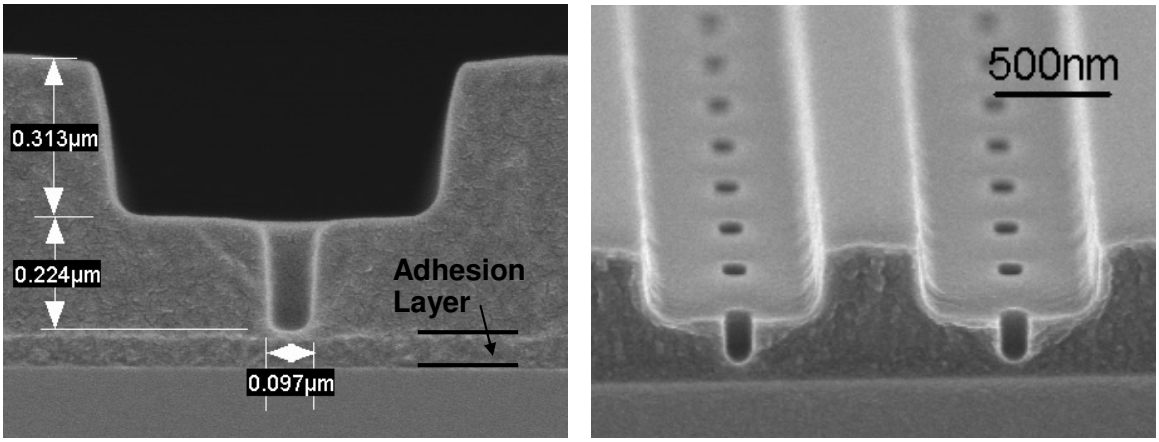
This chapter describes the development of multilevel the S-FIL process that was designed to maximize the yield of the via chain test vehicle. The critical S-FIL characteristics to be optimized turned out to be the residual layer thickness and the imprint uniformity. An ellipsometer technique was used in a non-destructive measurement of these imprint characteristics. Full wafer imprinting confirmed that the results were consistent.

9.2 PATTERN QUALITY

Imprint lithography is known to faithfully replicate the patterns on the fused silica template into the imprint resist layer. Figure 9.1 shows the multilevel patterns made by the multilevel S-FIL process in this study. In order to promote adhesion between the imprint resist and the wafer, an adhesion layer was required. The adhesion layer shown in Figure 9.1 (a) is BT-20 (Molecular Imprints, Inc., Austin TX) approximately 60 nm in thickness, which was coated at Molecular Imprints, Inc., Austin TX. The adhesion layer used in Figure 9.1 (b) was AP410 (Silicon Resources, Inc., Chandler AZ) coated at SVTC, Austin TX. Its thickness after the post application bake (PAB) was approximately 5 nm and is therefore barely discernible in Figure 9.1 (b). AP410 was used on the wafers for etch process development and electrical testing. BT-20 was used only in the early experiments conducted to verify the imprint pattern fidelity.

The via structures on the template were designed to be 120 nm, but provided reproducible imprinted via patterns ranging from 95 nm to 120 nm from place to place in

the patterns. This consistent variance very likely results from dimensional variation in the template features. The SEM images in Figure 9.1 show the excellent pattern quality produced by multilevel S-FIL. The imprinted via height is approximately 224 nm and line height 313 nm. This result is consistent with the AFM measurement of the feature height on the template reported in Table 8.3.



(a) (b)

Figure 9.1: Dual damascene features made with step and flash imprint lithography: (a) cross-section and (b) tilt-shot SEM (The adhesion layer shown in (a) was BT-20) – SEM courtesy of SVTC, Inc.

9.3 DROP PATTERN

The multi-droplet approach of monomer application was a significant breakthrough which enabled the achievement of the high throughput and low imprint force S-FIL process [9.2]. Faithful replication of the template pattern requires complete filling of the template contour without formation of air bubbles or extrusion at the edge of the template mesa. Figure 9.2 shows what incomplete filling looks like under the optical microscope on the S-FIL tool. Figure 9.2 was taken at the edge of the 1µm via

chain area on a Si test wafer as an example. In this study, the incomplete filling typically appeared on the via chains of large size (> 750 nm) that demand a high volume of liquid. This was subsequently confirmed by the electrical testing results described in Chapter 12.

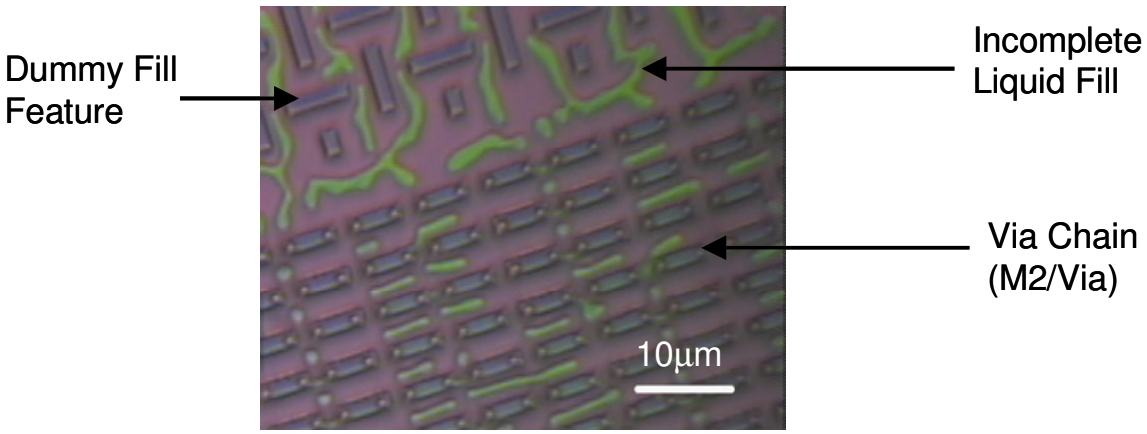
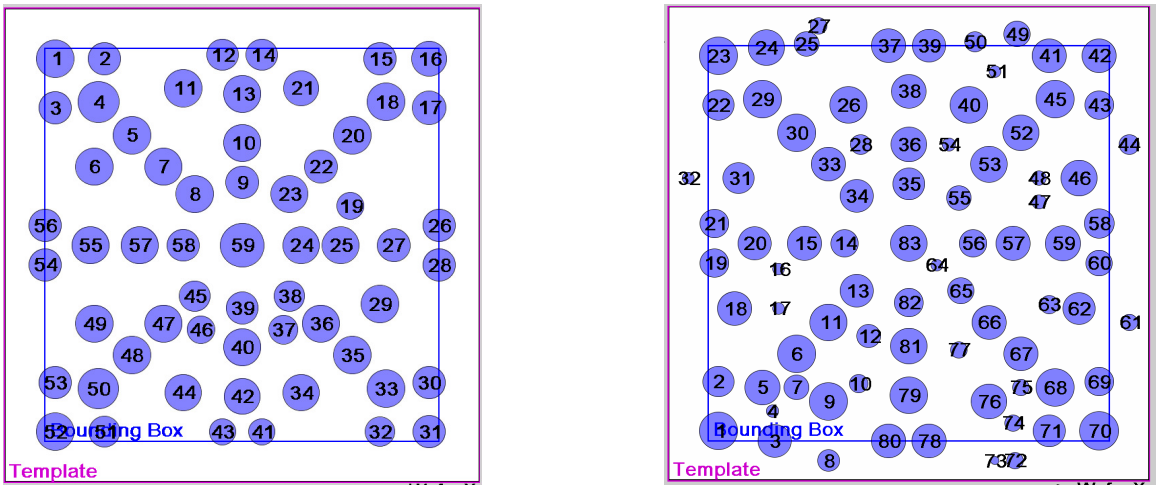


Figure 9.2: Typical incomplete filling of imprint liquids

The drop pattern is unquestionably the most important parameter controlling the filling process. The optimal droplet placement is very pattern specific [9.3,9.4] and therefore the advanced S-FIL tools are designed to automatically apply a drop pattern that is dictated by the mask pattern. However, optimization was conducted on a case by base manner for our tool set. In this study, a drop pattern was first developed to ensure complete liquid filling with a residual layer thickness of 50 nm. Figure 9.3 (a) shows the original drop pattern developed by Dr. Frank Palmieri and Kane Jen of the Willson Research Group. Figure 9.3 (b) shows the drop pattern that was improved in collaboration with Dr. Kang Luo and was subsequently used to produce the wafers for electrical testing. In Figure 9.3, the numbers indicate the sequence in which the drops

were dispensed and the sizes of the circles indicate the relative volume of the liquid droplets.



(a) (b)

Figure 9.3: Drop patterns: (a) original and (b) optimized for electrical testing

9.4 RESIDUAL LAYER THICKNESS (RLT) AND INTRA-DIE UNIFORMITY (IDU)

In addition to the pattern fidelity, the planarity of the imprint is also critical to maximizing the yield of the via chains on the test vehicle. It was indicated in Chapter 8 that the dual damascene template contains 4 identical quadrants. In order to show the uniformity of the imprint, SEM analysis was conducted at corresponding locations of the same imprint field (die). The result is shown in Figure 9.4 (a) through (d). These features were designed to be nominal 120 nm vias on the template. Figure 9.4 (e) shows the locations on the die where these images were obtained.

The residual layer is the imprint resist material under the via structure. After imprinting, the residual layer and the adhesion layer at the via pattern needs to be etched away to expose the underlying inter-level dielectric (ILD) material before the via pattern

can be transferred. Therefore a thin residual layer is usually preferred in imprint lithography. The via patterns are slightly rounded at the bottom. Therefore a slightly more stringent criterion for the feature height and thickness metrology was taken than that used in the preceding section. The via height was measured from the via entrance to the lower point of the vertical via sidewall and the residual layer thickness was from the lower end of the vertical via sidewall to the top of the adhesion layer, as indicated in Figure 9.4 (f). The rounded portion of the imprint resist must be etched away to fully expose the underlying ILD to subsequent etch chemistry. The more stringent metrology was therefore used for the integration requirements.

Based on the metrology depicted in Figure 9.4, the vertical portions of the via are consistent (201 nm to 206 nm). On the other hand, the residual layer thickness varies from place to place. Figure 9.4 shows a 67 nm variation of residual layer thickness, from 5 nm, Figure 9.4 (a), to 72 nm, Figure 9.4 (c). Since these SEM images were obtained from the center points of each quadrant, the whole field variation is expected to be even greater. This variation can affect the yield because the vias with the thickest residual layer might not receive sufficient etch to insure good electrical contact between the via and the M1 line after Cu is subsequently filled into the dual damascene features. Therefore the variance in residual layer thickness needs to be minimized.

In this study, intra die uniformity was defined as the standard deviation of the residual layer thickness measured on an imprint field (die). It represents the planarity of the imprinting process.

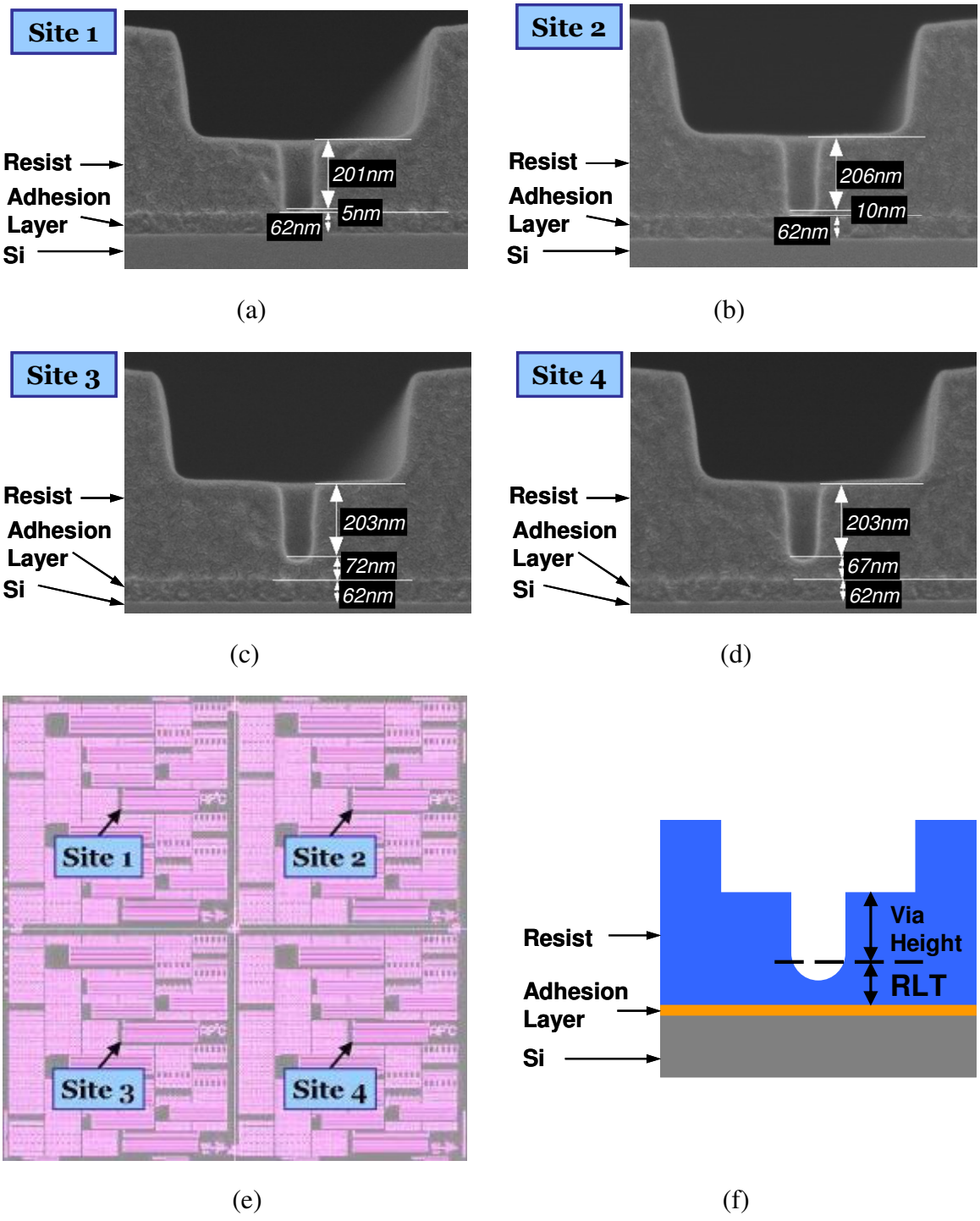


Figure 9.4: Uniformity of dual damascene imprint on one imprint field: (a) through (d) SEM images, (e) cross section locations, and (f) diagram for residual layer thickness (RLT) metrology – SEM courtesy of SVTC, Inc.

9.5 IMPROVEMENT OF INTRA-DIE UNIFORMITY (IDU)

When the template is brought into proximity of the wafer, a pressure is applied to the back of the template to control its curvature during imprint, as shown in Figure 9.5. This curvature of the template is intended to facilitate the liquid flow from the center to the edge of the field and thereby enhance imprint throughput and reduce potential entrapment of air bubbles. In the advanced tools, this back pressure can be dynamically controlled during imprint. Therefore, a high back pressure is applied when the liquid flows and fills the cavity on the template, and the back pressure is then reduced so that the template returns to planarity during photocuring of the imprint liquid. However, for our imprint tool, the back pressure can not be dynamically controlled. It remains constant during the imprint process. Therefore an additional experiment was conducted to find the back pressure that minimizes the intra die uniformity. This experiment was conducted in collaboration with Dr. Kang Luo.

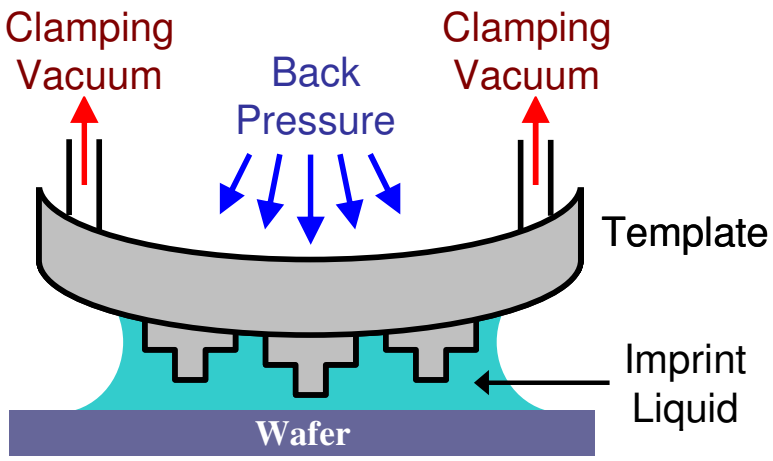


Figure 9.5: Effect of back pressure applied to the template during imprinting

9.5.1 Objective

1. To minimize intra die uniformity
2. To maintain low residual layer thickness (< 50 nm)

9.5.2 Experimental

The experiment was conducted with the Imprio-100 at Molecular Imprint, Inc., Austin TX using the drop pattern reported in Figure 9.3 (b). The metrology was conducted with a spectroscopic ellipsometer (KLA Tencor ASET-F5) at SVTC, Austin TX. The ellipsometer is equipped with an optical microscope and pattern recognition software. Therefore it can locate a prescribed position on the pattern and measure the film thickness with lateral geometries as small as a few tens of microns. In this study, we measured the thickness at the 120 μm square probe contacts. These contact patterns are at the Metal 2 line level of the dual damascene template. The actual residual layer thickness can therefore be derived by subtracting the fixed via height from the line level thickness. Figure 9.6 shows the relationship between the line level measurement and the residual layer thickness.

The ellipsometer measurement was calibrated by SEM analysis at the same locations, and the calibration plot is shown in Figure 9.7. It was found that the thickness indicated by the ellipsometer measurement is on average 30 nm thicker than the SEM analysis. Subsequent ellipsometer measurements were adjusted accordingly.

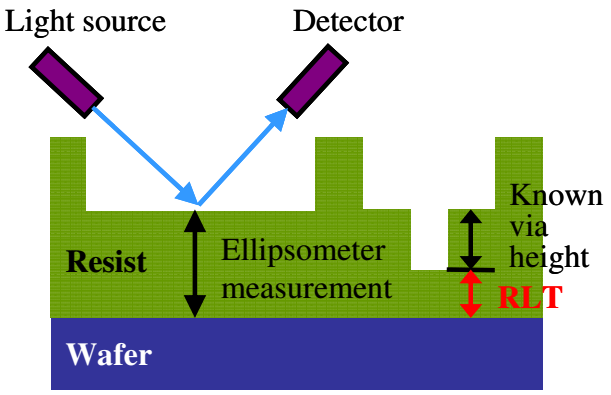


Figure 9.6: Measurement of imprint uniformity using ellipsometry

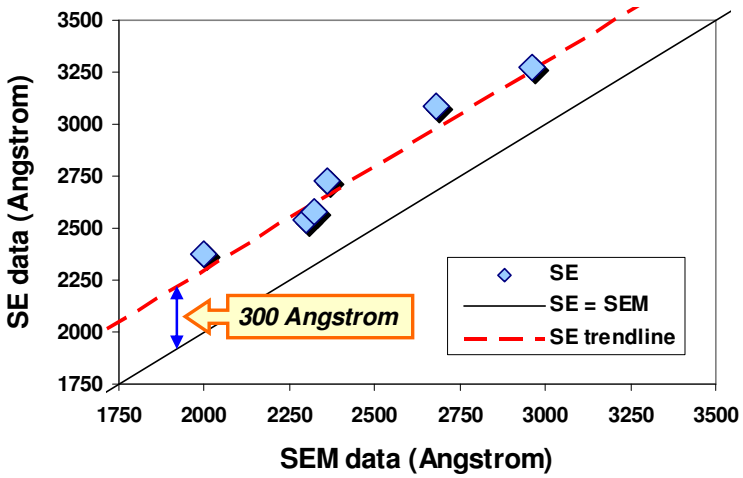


Figure 9.7: Ellipsometer measurement correction curve based on SEM analysis

Figure 9.8 shows ellipsometer measurement location in each tested imprint field. Residual layer thickness was measured with ellipsometer at 17 locations that include the center point, corners and mid points of the outer edge and mid points between center and edge points.

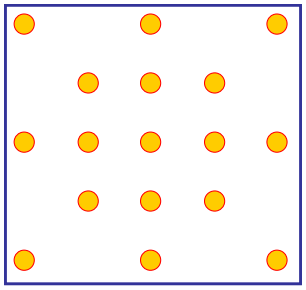
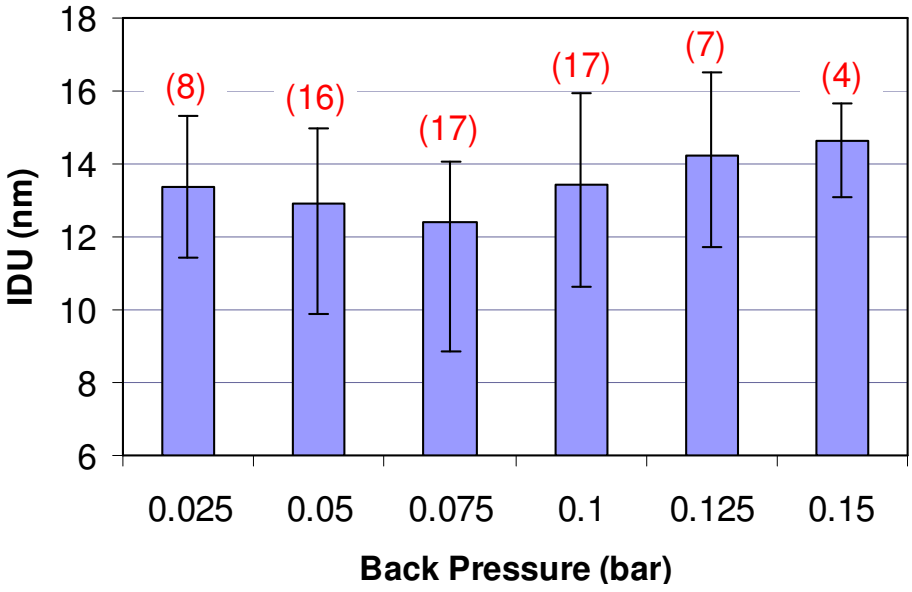


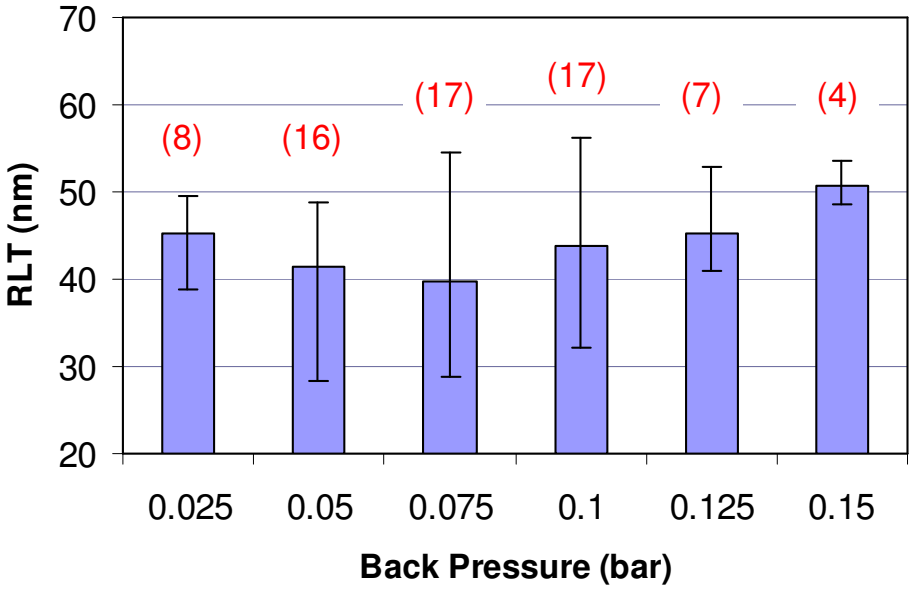
Figure 9.8: Ellipsometer measurement locations on each imprint field

9.5.3 Results and Discussions

Intra die uniformity was optimized by adjusting the back pressure while keeping other factors constant. Figure 9.9 shows the resulting intra die uniformity with respect to the back pressure. Both the residual layer thickness and intra die uniformity reached their minima at back pressure 0.075 bar. At this back pressure, the average intra die uniformity was 12.4 nm 1σ. This condition was subsequently used in full wafer imprinting for electrical testing.



(a)



(b)

Figure 9.9: ILD and RLT variation with respect to back pressure: (a) IDU, and (b) RLT (the number of data points was labeled above the variation bars in red.)

9.6 FULL WAFER IMPRINTING

Full wafer imprinting was conducted using the process developed above. An IDU below 15nm 1σ was achieved consistently in our imprint process and this provided good via chain yield, which is reported in Chapter 12. Figure 9.10 shows the intra die uniformity measurement of a fully imprinted wafer. The edge die typically have poorer intra die uniformity. This is likely due to problems with leveling of the wafer chuck on the imprinter. Therefore, all 37 die were imprinted on each wafer for electrical testing, however, only the center 21 die (excluding the edge die) were tested.

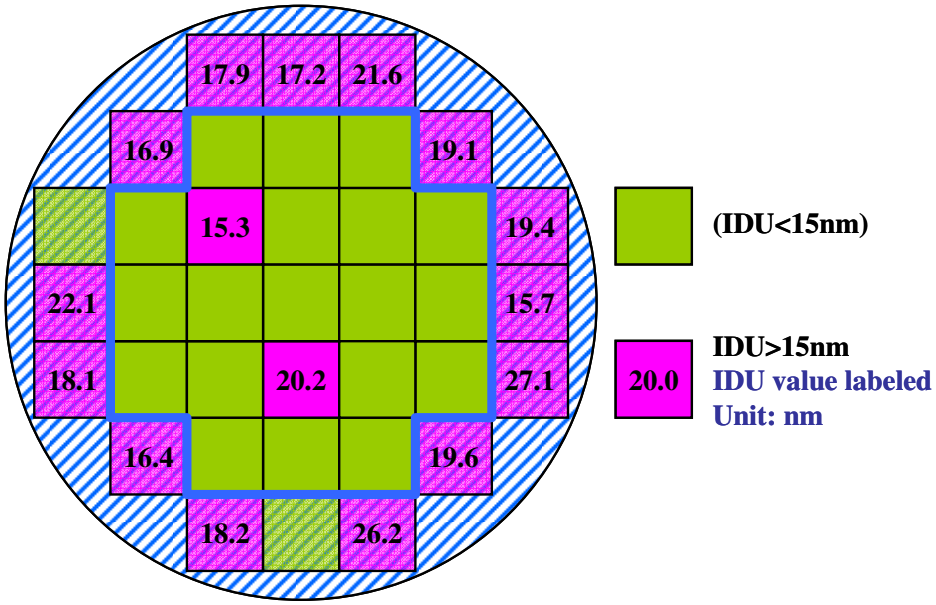


Figure 9.10: Wafer map of IDU variation

9.7 CONCLUSIONS

For the advanced S-FIL tools, the drop pattern dictated by the mask pattern can be automatically generated and the back pressure can be dynamically controlled to produce uniform imprints. Unfortunately these sophisticated functions are not available on the tool set used in this study. Therefore, experiments in drop pattern and back pressure were conducted to develop an imprint process that insures complete liquid filling and produces very uniform imprints.

Chapter 10: Pattern Transfer I – Process Development

10.1 INTRODUCTION

Chapter 9 describes a high fidelity Step and Flash Imprint Lithography (S-FIL) process to make multi-level dual damascene patterns. This chapter describes the reactive ion etching (RIE) process that was developed to transfer the dual damascene patterns from the imprint resist into the underlying low dielectric constant (low-k) inter-level dielectrics (ILD). With Multi-level dual damascene imprint the via and the line level patterns are printed simultaneously into the same resist layer. This poses significant challenges in developing an etching process that must conserve the multilevel profile of the imprint. Development of the multi-level pattern-transfer etch is key to the success of the integration of S-FIL into the dual damascene processing flow.

10.2 ETCHING SELECTIVITY

In the early development, the strategy was to search for a material and an etching chemistry that provide the same etch rates for the resist and the dielectric materials. The hope was that 1:1 etch rates would transfer the feature patterns from the imprint into the ILD layer exactly and in one single etching step. This can also be expressed as the etch selectivity in Equation (10.1).

$$S = \frac{R_{ILD}}{R_R} = 1 \tag{10.1}$$

where R_{ILD} is the etch rate for ILD and R_R is the etch rate for the resist material.

A simplified etch selectivity simulation was conducted in order to obtain a general understanding of the correlation between the etch selectivity and the evolution of the feature profile. The program was written with Matlab R2005. The material stack includes, from top to bottom, the imprint resist, an adhesion layer, low-k ILD, and cap layer. No specific materials were assigned and the only factor considered is the relative etch rates of each layer. The result is shown in Figure 10.1.

Figure 10.1 (a) shows that the etched feature conserves the profile of the resist feature when the etch rates of resist and ILD are comparable, that is, S=1. Figure 10.1 (b) shows that the feature will be shortened when the chemistry has higher etch rates for resist than it has for the ILD, that is, S<1. The results of both Figure 10.1 (a) and 10.1 (b) are independent of the etch rate of the adhesion layer, as long as the feature has been fully etched into the ILD.

In order to maintain or increase the aspect ratio of the imprinted feature, the desirable condition is clearly S>1. Figure 10.1 (c) shows a simulated case of S=2. In this case, the via height of the final feature did not extend to twice the height of the original resist feature. This is because the Metal 1 Cu under the cap layer is inert to the dielectric etching chemistry. The via etching effectively stops once the cap layer at the via bottom is broken through and the Metal 1 Cu is exposed. Therefore, the via height is actually controlled by the etch depth at the line level. This simulation result indicates that there is a process window to control via height for an etch chemistry that has S>1.

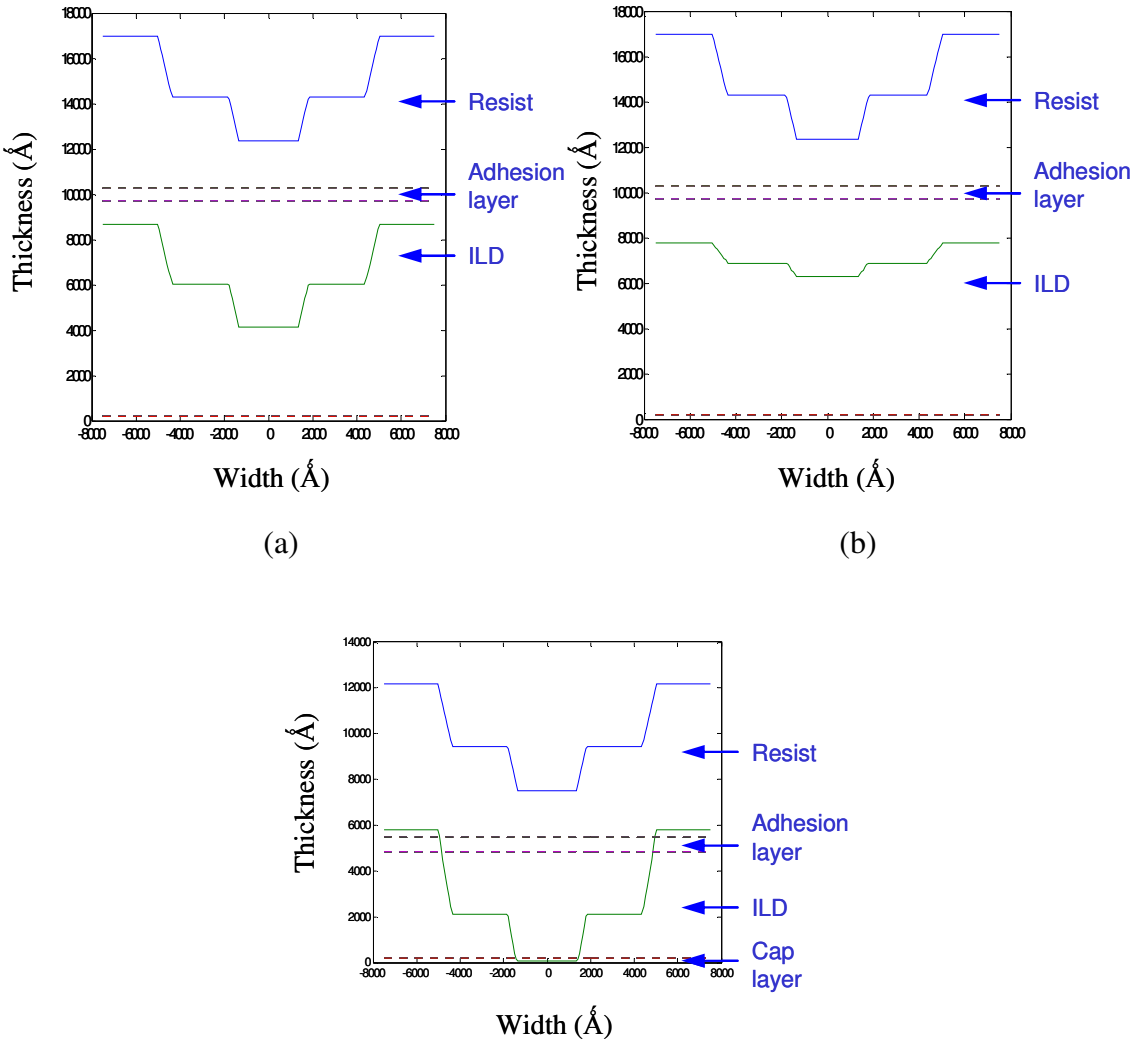


Figure 10.1: Etch selectivity simulations. (a) $R_R = R_{ILD}$, (b) $R_R > R_{ILD}$, and (c) $R_R < R_{ILD}$. (R_R = etch rate of imprint resist, R_{ILD} = etch rate of ILD; the blue lines indicate resist profiles and the green lines indicate the feature profile after etch)

10.3 CHALLENGES IN MULTILEVEL TRANSFER

In addition to the selectivity, other critical restrictions apply to the pattern transfer etching, such as etch anisotropy as shown in Figure 10.2. Dielectric etching in microelectronics is mostly conducted in ion-enhanced, fluorine-based plasma systems. Vertical profiles are achieved by sidewall passivation, typically by introducing carbon-containing fluorine species into the plasma [10.1], as reviewed in Section 7.3. The etching chemistry has profound impact on the final profile of the etched features. Two major challenges were identified during the development of the S-FIL etch process: etch artifacts and residual layer uniformity in the imprint patterns. They are shown in Figure 10.3 and described in the following sections. The proposed approach to solve these issues is discussed in Section 10.4.

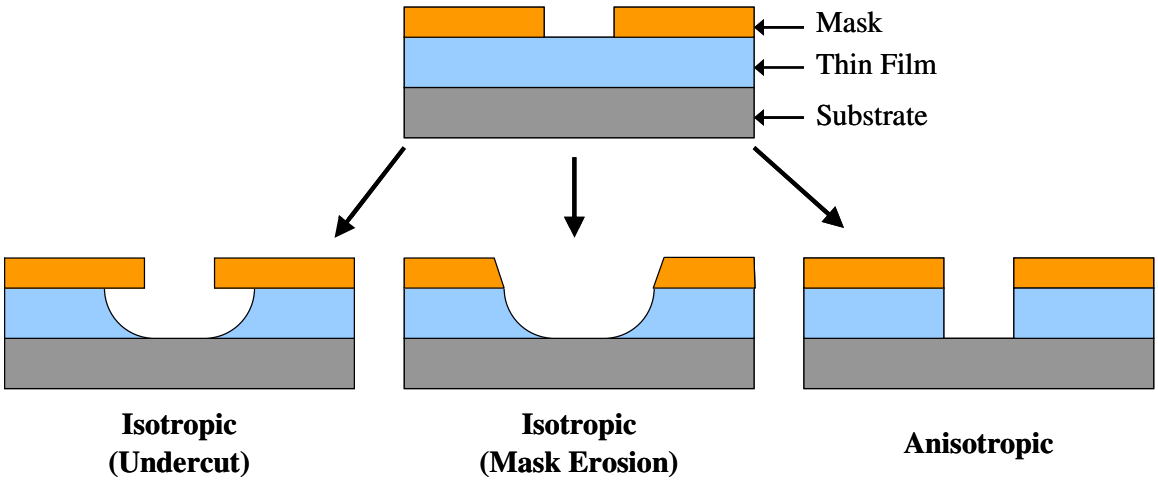


Figure 10.2: Isotropic and anisotropic etching profiles

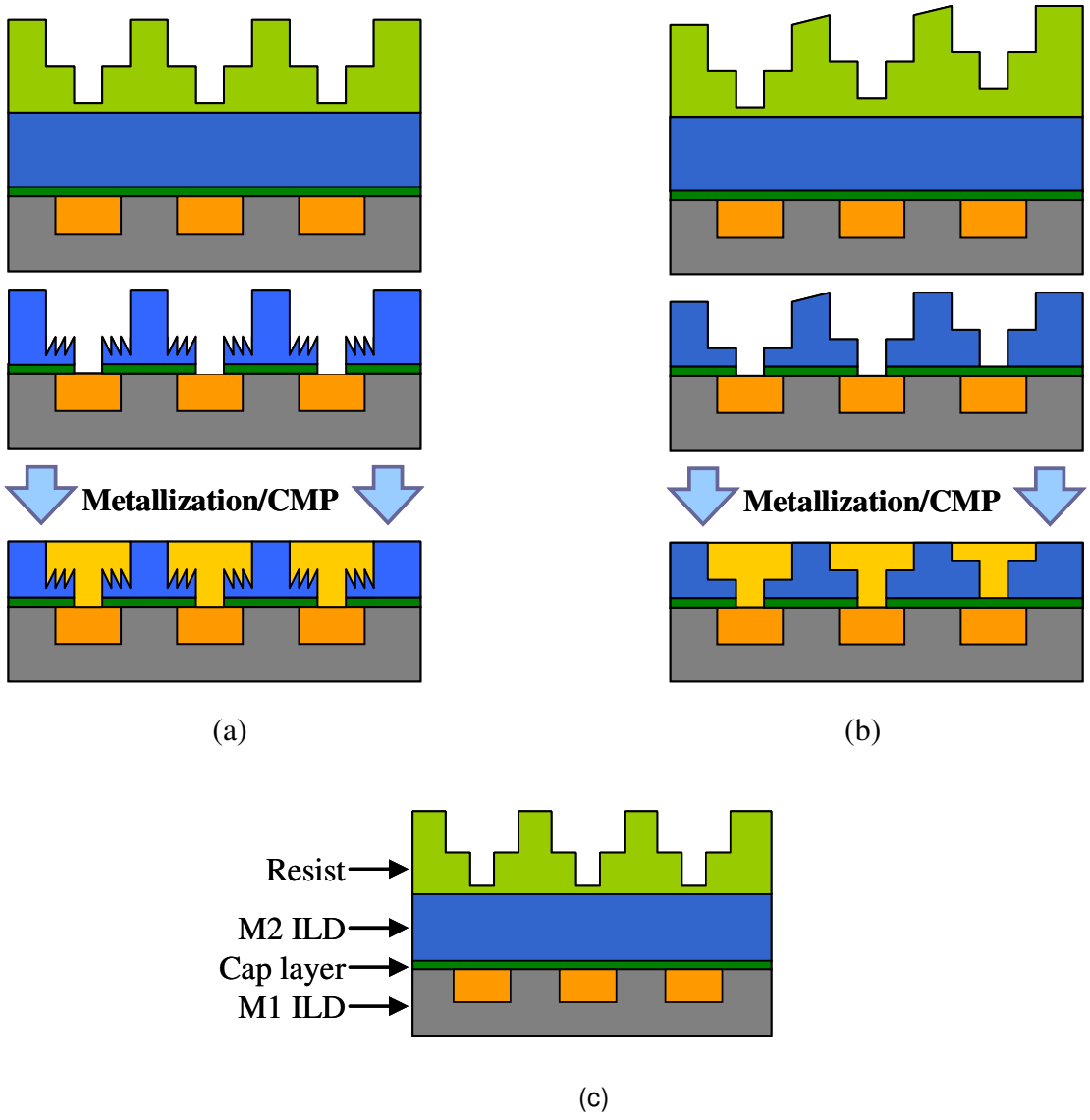


Figure 10.3: Challenges in pattern transfer etch for multilevel S-FIL: (a) etch artifacts, and (b) imprint uniformity (note that the wire on the right has reduced cross section and it is not successfully connected to M1); (c) diagram legends

10.3.1 Etch artifact

In order to achieve the anisotropic etching required for patterning features with vertical sidewalls, highly polymerizing etching chemistry was employed. Such chemistry generally renders a very rough top surface on the resist due to concurrent etch residue deposition and aggressive ion bombardment. In the photolithographic process, the via and line structures are patterned separately. The resist over the protected area is never consumed during pattern transfer and therefore the undesirable etch artifacts do not affect the etched features. For multilevel S-FIL, the resist at the line level protects the dielectrics when the via structures are being transferred. However, the line level resist must be subsequently consumed in order to transfer the line patterns. Etch artifacts and surface roughness that accumulate on the resist can therefore be transferred into the dielectric during the line etch as described in Figure 10.3 (a). Figure 10.4 is an image obtained in an early experiment showing this effect. Significant roughness formed on the the line level resist that was transferred into the dielectrics causing the undesirable etched feature indicated in Figure 10.3 (a). These etch artifacts can compromise the performance and reliability of the Cu interconnects, and must therefore be eliminated.

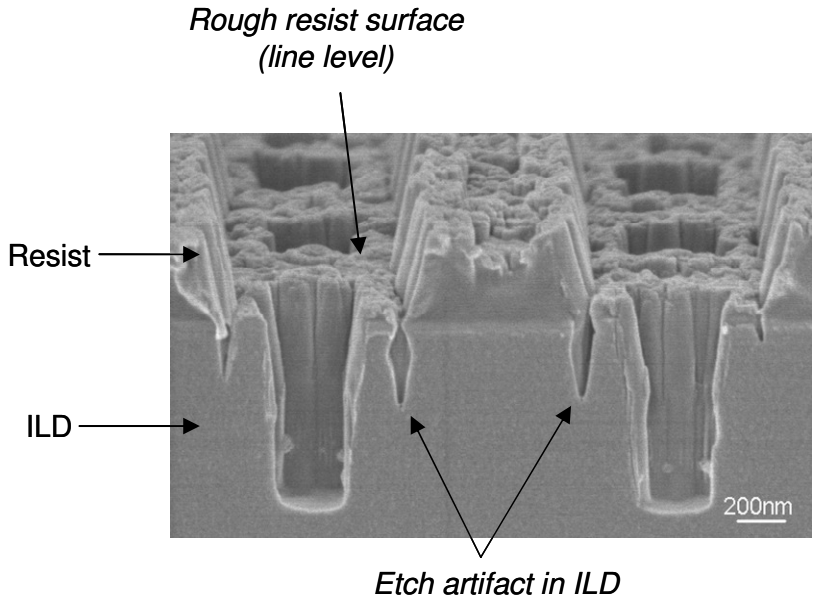


Figure 10.4: Etch artifacts – SEM courtesy of SVTC, Inc.

10.3.2 Imprint Uniformity

Process-induced variations in interconnect geometry have a profound impact on the performance of high speed processors. Interconnect geometry variation causes clock skew variability and substantially compromises performance and production yield [10.2]. For the conventional process, the most common intra-die variation is due to line CD variation that results from optical proximity effects and feature height variation, which in turn is a result of variations in CMP dishing and erosion rates that vary with pattern size and density [10.3,10.4].

In multilevel S-FIL, line height variation can also be caused by variance in the residual layer thickness. Its potential impact on the interconnect geometry is shown in Figure 10.3 (b). In the extreme, if the initial residual layer is too thick, some areas may not receive sufficient etching to penetrate the cap layer, leading to low via yield.

Therefore, an ideal etching process needs to be able to tolerate a certain budget of residual layer thickness variance. Figure 10.3 (b) shows the imprinted profile of three dual damascene features taking into account the variance in residual layer thickness of the imprint. In an actual imprint, features with various residual layer thicknesses are far away from each other on the imprint field, rather than adjacent to each other. In Figure 10.5 (a), these features were drawn next to each other in order to demonstrate the effects of such variance.

10.4 MULTI-STEP ETCH SCHEME

An *in-situ*, multistep etch scheme was developed to achieve faithful pattern transfer of the multilevel imprints and meet the etching challenges described in the previous section. Figure 10.5 shows a diagram depicting each step of the proposed multi-step etch scheme. The goals and requirements of each step of the etch scheme are detailed below.

Step 1: residual layer open

Figure 10.5 (b) shows a diagram depicting the intended result of the residual layer open step. This etch step opens the thin residual layer at the bottom of the via. The chemistry in this step must have high selectivity of resist over ILD. The high selectivity enables elimination of any variation at the via level. This step must open all vias while leaving sufficient resist thickness to support subsequent steps.

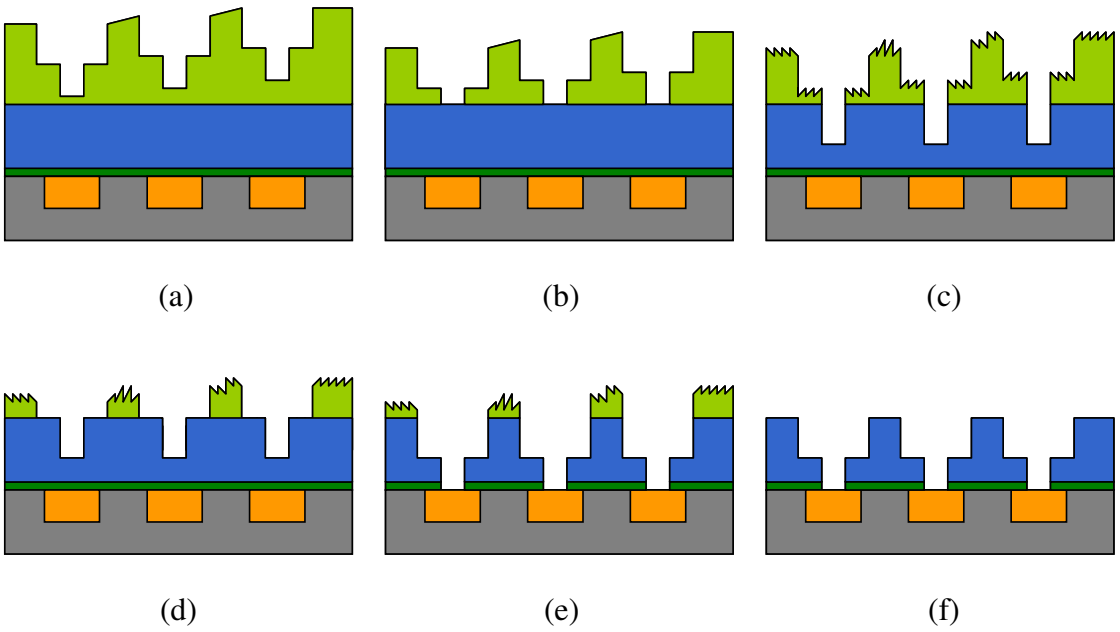


Figure 10.5: Multi-step etch scheme. (a) Imprint, (b) residual open, (c) via etch, (d) line descum, (e) line etch, and (f) resist ash

Step 2: Via transfer

Figure 10.5 (c) shows a diagram depicting the intended result of the via transfer step. The purpose of this step is to transfer the via pattern into the ILD. In order to achieve optimal via sidewall slope, use of highly polymerizing chemistry is required. However, highly polymerizing chemistry generates a very rough top surface on the resist. This produces resist surface roughness at the line structures, as described in Section 10.3.1. Therefore, control of the roughness at the line level is critical. The via transfer step must be terminated well before the undesirable etch artifacts are transferred into the ILD.

Step 3: Line descum

Figure 10.5 (d) shows a diagram depicting the intended result of the line descum step. The line descum step prevents the etch artifacts generated at the via etch step from being transferred into the ILD. Therefore, the ideal chemistry should have high resist etch rate and selectivity relative to the ILD. An advantage of this etch step is that any non-uniformity in the line patterns that originated from the imprinting is removed as the line pattern transfer etch will start on the smooth and planar ILD surface.

Step 4: Line transfer

Figure 10.5 (e) shows a diagram depicting the intended result of the line transfer step. The line transfer step must not only transfer the line pattern but also maintain the fidelity of the via pattern. An additional but important role of the line etch is to breakthrough the cap layer to expose the Metal 1 Cu.

Step 5: Ash

Figure 10.5 (f) shows a diagram depicting the intended result of the final ash step. After the line etch step, the multilevel dual damascene pattern is transferred. The final ash step must strip the remaining imprint resist without oxidizing the exposed Metal 1 Cu at the via bottom. The imprint resist is an organic polymeric material. Therefore, standard H_2/N_2 ash processes used to strip photoresist can be used in this step.

10.5 PATH FINDING EXPERIMENTS

In order to identify the proper etching chemistry for each step, a set of path finding experiments was conducted based on the gases that were available on the plasma etcher. The design of the experiments is shown in Figure 10.6. It is important to note that the processing conditions were not optimized while conducting these experiments. The purpose of the experiments was simply to identify promising candidates to facilitate further exploration. In Figure 10.6, critical experiments are labeled (b) to (h), which correspond to the experimental results in Figure 10.7 (b) to (h). The results of these experiments are discussed in further detail in the following section.

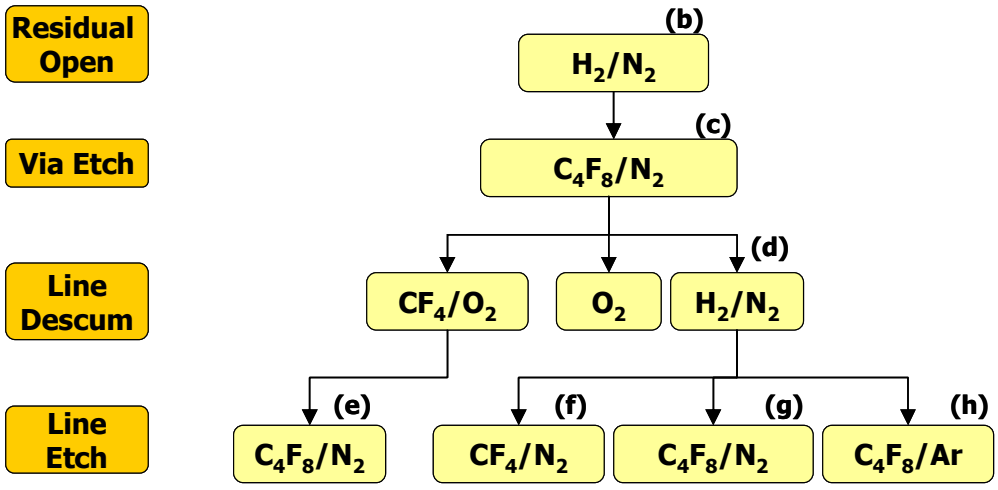


Figure 10.6: Design of path finding experiment for pattern transfer etch

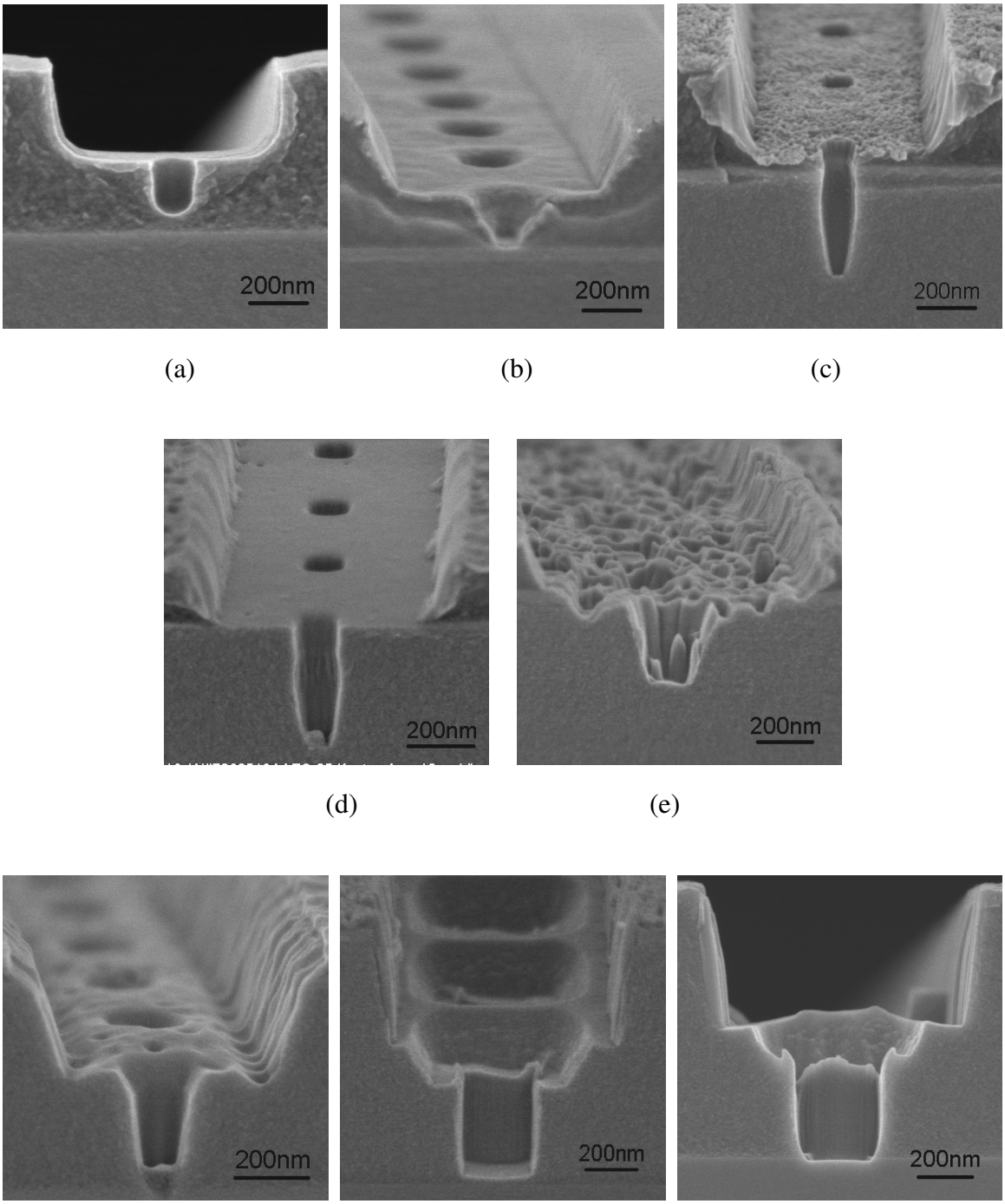


Figure 10.7: Critical results in path finding experiment. (a) Imprint, and (b) through (h) as labeled in Figure 10.6 – SEM courtesy of SVTC, Inc.

10.5.1 Apparatus

All etch experiments in this study were conducted using a Tokyo Electron Unity II E etcher equipped with two Dual Ring Magnet (DRM) chambers in the facility of SVTC in Austin, Texas. The reaction gases installed on the equipment include CF_4, C_4F_8, CH_3F, Ar, H_2, N_2, CO, and O_2.

10.5.2 Results and Discussion

10.5.2.1 Residual Open

Figure 10.7 (b) shows a 120 nm via structure after the residual-open step using H_2/N_2 chemistry. This chemistry achieved the process objective of this etch step. After breaking through the residual layer, etching automatically stops at the via bottom on the ILD surface because H_2/N_2 has very high resist-to-ILD selectivity. Due to the non-polymerizing characteristics of the etch gas, the resist surface remained smooth, however, sidewall slant was induced. The sidewall slant is not a desirable feature. However, we have found that the final profile still has vertical sidewall after the all etch steps were completed even if the sidewall slant occurred in the residual open step. Therefore, we did not optimize this step to have vertical sidewalls.

10.5.2.2 Via Etch

The via etch step is designed to transfer the via pattern from the resist into the ILD. A polymerizing chemistry is needed to make the via sidewall vertical. $C_4F_8/Ar/N_2$ chemistry was found to be appropriate, requiring only a minor modification to a standard SVTC recipe. The result is shown in Figure 10.7 (c). The via was

vertical but the resist surface was rough due to the polymerizing chemistry used. Therefore, the via etch process must be terminated before the etch artifacts are transferred into the ILD.

10.5.2.3 Line Descum

Two chemistries were considered: H_2/N_2 and CF_4/O_2. H_2/N_2 chemistry was considered first because this step is very similar to the residual open step. The result of H_2/N_2 chemistry is shown in Figure 10.7 (d). The surface of the trench (line) was very smooth and no surface artifacts were transferred to the ILD.

Figure 10.7 (e) shows the result of an experiment that was conducted using CF_4/O_2 chemistry. This chemistry is aggressive to both resist and ILD and therefore etch artifacts were transferred from the resist into ILD. The result was not acceptable. Therefore, H_2/N_2 was chosen as the chemistry to be used in the line descum step.

10.5.2.4 Line Etch

After the line descum step, the wafer was subjected to the line etch step to transfer the line patterns of the dual damascene feature into the inter-level dielectrics. The line etch needs to conserve the vertical profile of the via while faithfully transferring the line patterns. Development of the line etch process was substantially more challenging than previous steps. It is the last etching step before removing the resist completely. Therefore, this step determines the final feature profile. Both CF_4 and C_4F_8 chemistries were considered for this step. Early results are shown in Figure 10.7 (f), (g), and (h). It is obvious that neither of these systems provided the ideal profile. The feature in Figure 10.7 (f), generated with CF_4, has undesirable sidewall angles at both the via and

the line levels. The features in Figure 10.7 (g) and (h), that were generated with C_4F_8, show substantial faceting at the via entrance. Development of the proper line etch chemistry is given in Section 10.6.

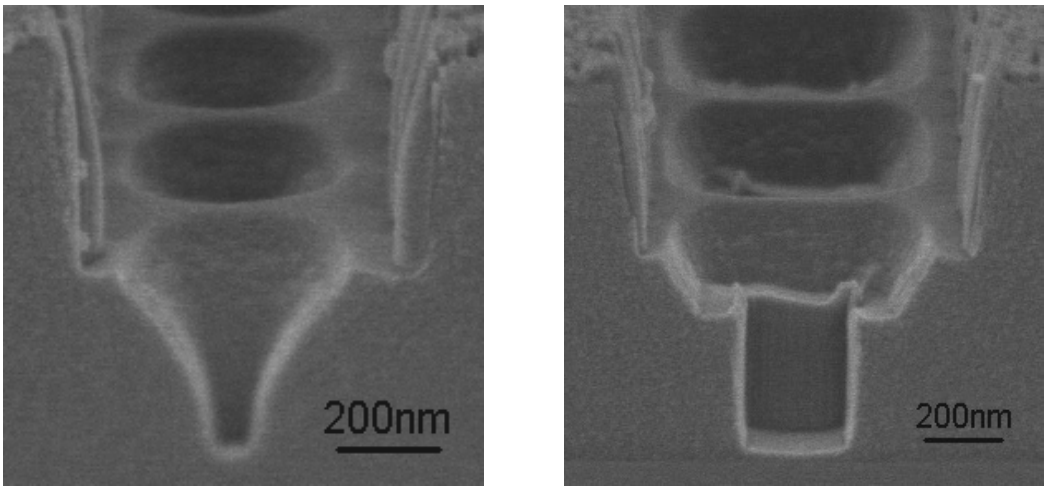
10.5.2.5 Ash

The purpose of the ash is to strip the remaining resist after completion of the pattern transfer. H_2/N_2 chemistry was used in this study because it does not oxidize the Metal 1 Cu exposed at the via bottom.

10.6 FACET FORMATION

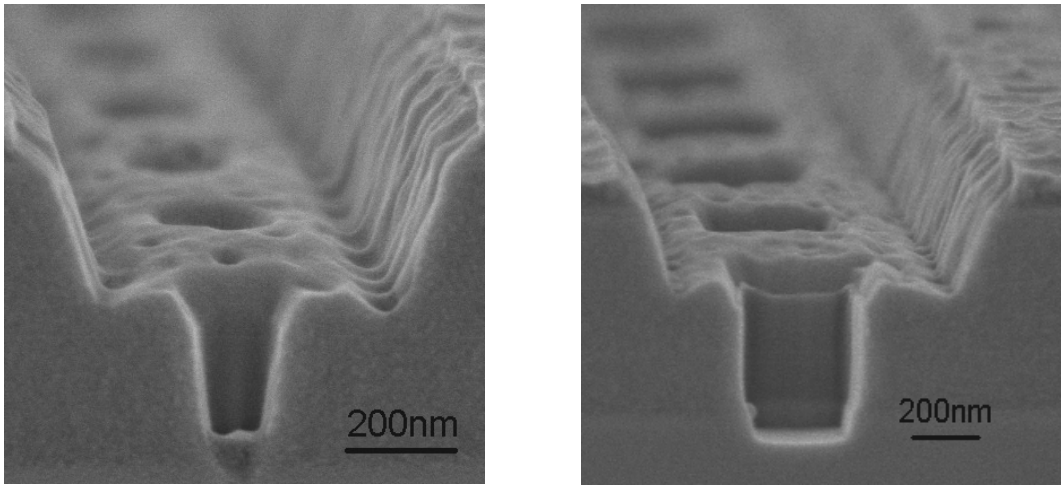
10.6.1 Challenges

As indicated in Figure 10.6 and Figure 10.7, line etch based on the two most common etch chemistries C_4F_8 and CF_4 was tested first. The results are shown in Figure 10.8 and Figure 10.9 respectively. Figure 10.8 shows that C_4F_8 chemistry renders very vertical sidewalls at the line level. However, significant facet formation at the via entrance compromises the via critical dimensions. It was also consistently observed that the smaller the via feature, the more severe the facet formation at the via entrance. This is obviously an unacceptable result. With CF_4 chemistry, as shown in Figure 10.9, facet formation was much more subdued whereas the via profile was undesirable and there was surface roughness, and micro-trenching. Both C_4F_8 and CF_4 chemistries transfer the patterns from the resist into ILD, however each has distinct shortcomings. Because C_4F_8 chemistry has greater potential providing vertical sidewalls, the following development was based on this chemistry and focused on reducing the via faceting generated by this chemistry.



(a) (b)

Figure 10.8: Line etch using C_4F_8 chemistry: nominal via critical dimensions: (a) 120 nm, and (b) 250 nm – SEM courtesy of SVTC, Inc.

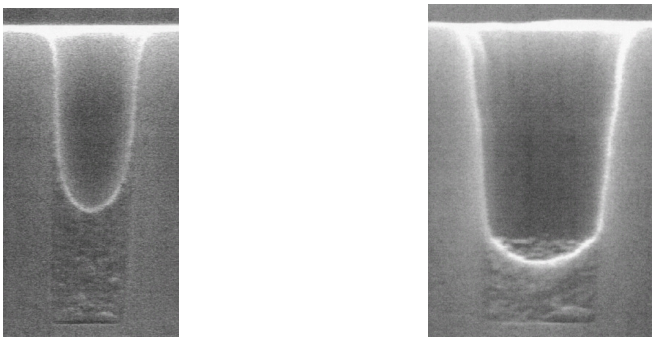


(a) (b)

Figure 10.9: Line etch using CF_4 chemistry: nominal via critical dimensions: (a) 120 nm, and (b) 350 nm – SEM courtesy of SVTC, Inc.

10.6.2 Facet/Fence Formation in BEOL Processing Using Photolithography

Before describing the solution to the facet formation problem encountered in this study, it might be useful to extend a brief review of the similar problem in dual damascene processing using photolithography. Facet and fence formation are the major challenge in the line etch process in the standard photolithographic BEOL process. Research showed that the bottom antireflective coating (BARC) filled in the via structure can play an important role in controlling the facet/fence formation [10.5]. A BARC is a layer of polymeric film with carefully designed optical properties and thickness, which is applied to prevent standing waves during photolithography exposure. Figure 10.10 shows the BARC meniscus inside a via prior to the line etch step. When the BARC meniscus and filled height are managed appropriately, the BARC protects the via sidewall from the line etch chemistry, and formation of via faceting or fencing can be prevented [10.5].



(a) (b)

(Source: D. L. Keil, B. A. Helmer and S. Lassig in Ref [10.5])[9]

Figure 10.10: BARC meniscus in the via using photolithography. (Length scale was not provided in the original images.)

[9] Reused with permission from D. L. Keil *et al*., Journal of Vacuum Science & Technology B, 21, 1969 (2003). Copyright 2003, AVS: Science & Technology of Materials, Interfaces, and Processing.

The following discussion regarding the BARC/faceting interaction in the dual damascene etch process is based on the review made by Keil *et al*. [10.5]. Figure 10.11 shows an ideal line etch process. The dotted line in Figure 10.11 (a) indicates the intended line height. When a thick BARC is used, as shown in Figure 10.12 (a), a veil-like feature can form at the via entrance. This is because BARC usually has etch characteristics similar to photoresist. Therefore the dielectrics surrounding the thick BARC receive reduced exposure to the etching radicals. The result can be more pronounced when the via is tapered due to the additional shadowing effect. Figure 10.13 shows the facet formation when a thin BARC is used. Without the protection of BARC, the feature is susceptible to the preferential etching at the top corner of the via [10.6]. In addition to these two conditions, Keil *et al*. [10.5] also showed other BARC/etch interactions that facilitate facet or fence formation during the line etch of dual damascene features. Figure 10.14 shows examples of facet formation due to the BARC/etch interaction [10.5].

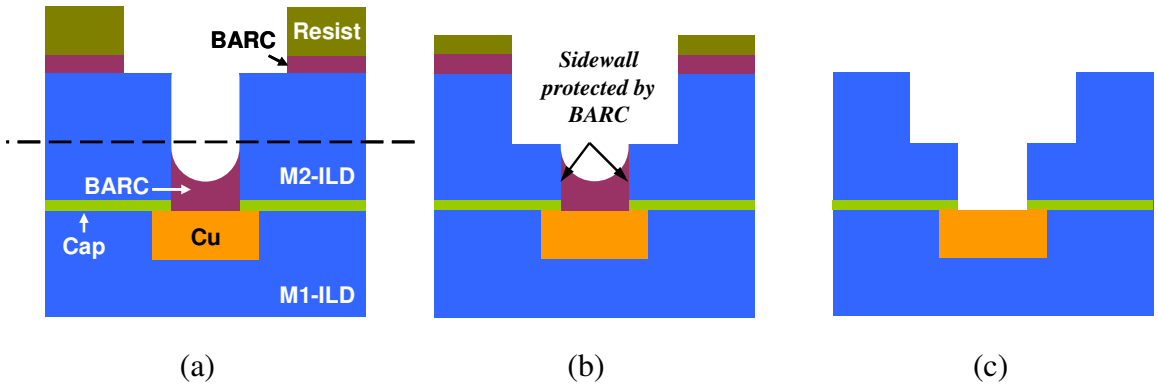


Figure 10.11: Ideal line etch process in standard, photolithographic dual damascene processing. (a) before line etch, (b) after line etch, and (c) after resist strip (This diagram was drawn by the author based on the discussion in Ref [10.5])

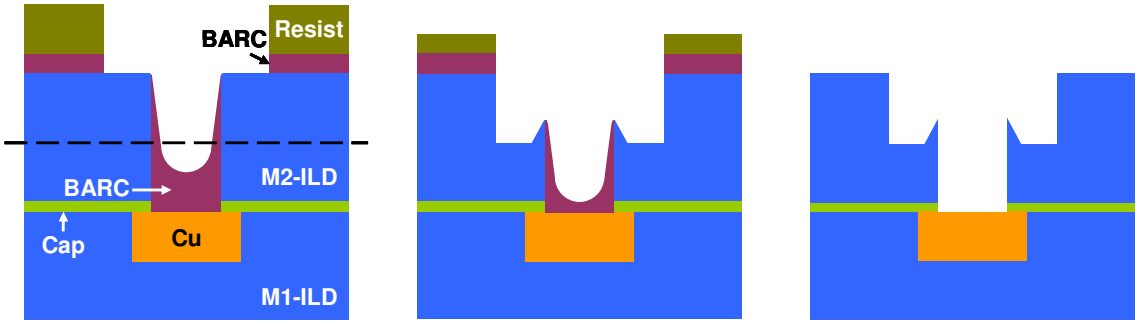


Figure 10.12: Fence formation at via entrance due to "via underfill" of a thick BARC inside the via: (a) before line etch, (b) after line etch, and (c) after resist strip (This diagram was drawn by the author based on the discussion in Ref [10.5])

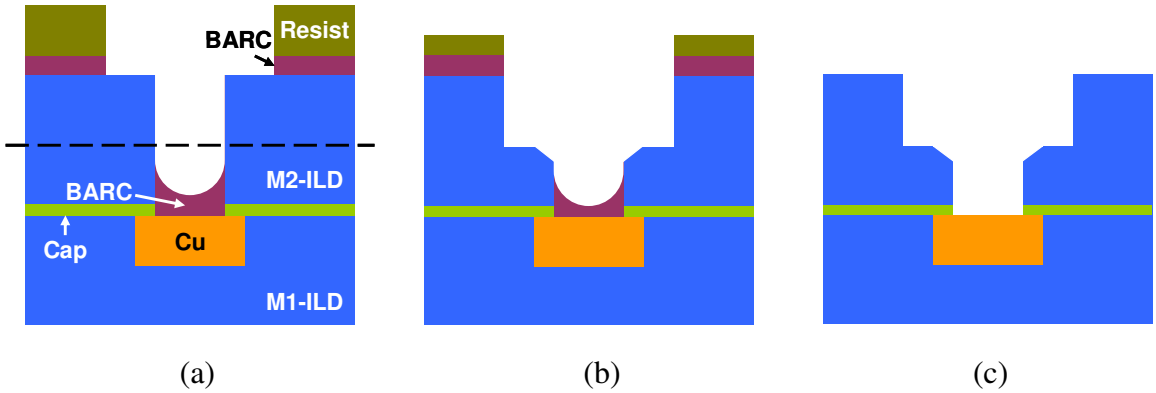
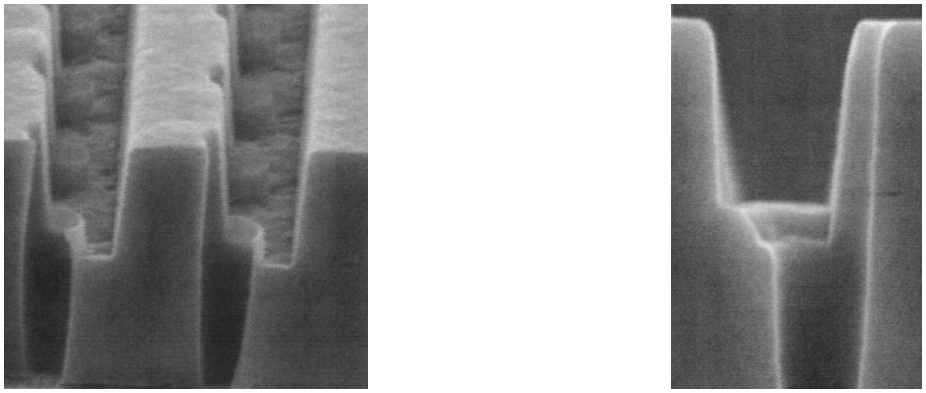


Figure 10.13: Facet formation at via entrance due to "via underfill" of a thin BARC inside the via (This diagram was drawn by the author based on the discussion in Ref [10.5])



(a) (b)

(Source: D. L. Keil, B. A. Helmer and S. Lassig in Ref [10.5])[10]

Figure 10.14: (a) Fence formation and (b) facet formation due to interaction between etch chemistry and BARC meniscus inside the via. The misalignment is irrelevant to the discussion of etch process. (Length scale was not provided in the original images.)

The fence and facet form through complex mechanisms. The description given above is only a general discussion of the problem. The strategies needed to suppress these artifacts are varied and often application dependent [10.6]. The intended function of BARC is to reduce the standing wave effect in photoresist during exposure. Therefore it usually is impractical or impossible to attempt control of the BARC meniscus and fill height to suppress facet or fence formation.

In light of the difficulty in integrating BARC into a line etch process, Intel introduced a new approach that employs a new material they call SLAM (Sacrificial Light Absorbing Material) [10.7]. Figure 10.15 shows the line etch step of SLAM assisted dual damascene patterning process. SLAM is an opaque film, which completely fills the vias and covers the wafer surface when the line patterns are imaged

[10] Reused with permission from D. L. Keil *et al.*, Journal of Vacuum Science & Technology B, 21, 1969 (2003). Copyright 2003, AVS: Science & Technology of Materials, Interfaces, and Processing.

with photolithography. Its etch characteristics are similar to that of the ILD. Facet and fence formation are therefore reduced or eliminated because the etch rate of the via fill material matches that of the surrounding dielectrics. However, Intel did not explain how SLAM was selectively removed after the line etch was completed.

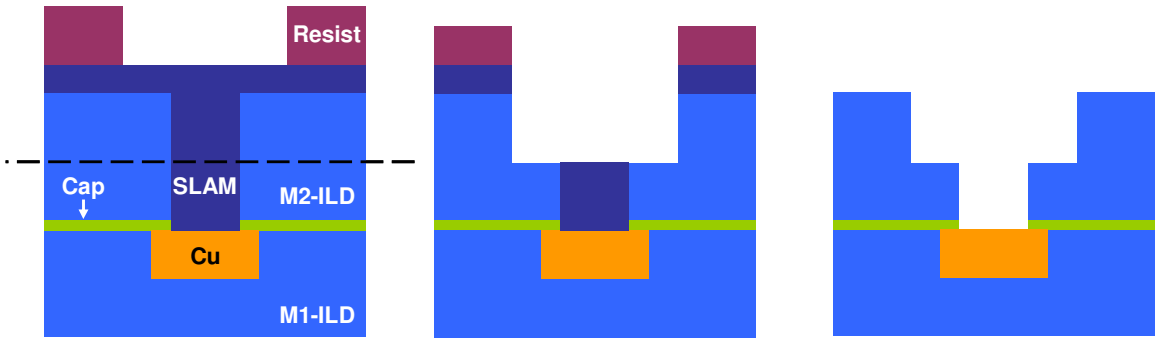


Figure 10.15: SLAM assisted line etch process for dual damascene patterning (This diagram was drawn by the author based on the discussion in Ref [10.7])

10.6.3 Facet/Fence Formation in BEOL Processing Using Multilevel S-FIL

Figure 10.16 shows the ideal line etch process for multilevel S-FIL. It is apparent that the lack of a via fill material, BARC or SLAM, causes the top corner of the via to be directly exposed to the attack of both chemical and physical etching species. Due to the preferential physical sputtering at the exposed corner, as shown in Figure 10.17, there is a strong proclivity for a via facet to form during line etch, as shown in Figure 10.18. This is confirmed by the early experimental results shown in Figure 10.8.

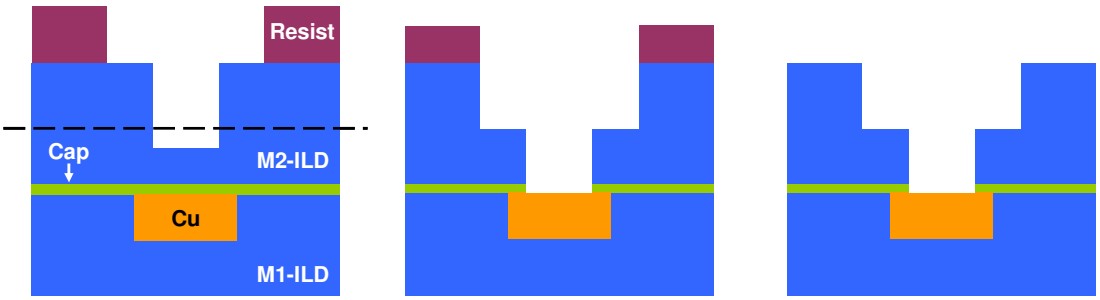


Figure 10.16: Ideal line etch process for multilevel S-FIL

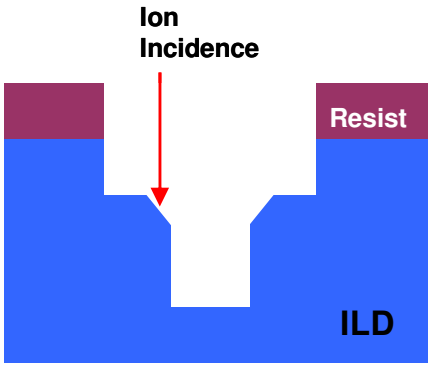


Figure 10.17: Preferential etch at the corner

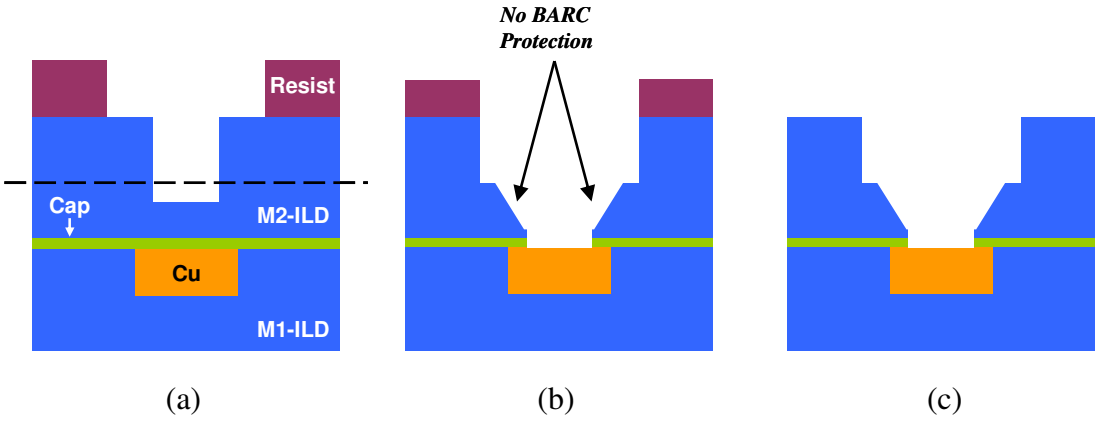
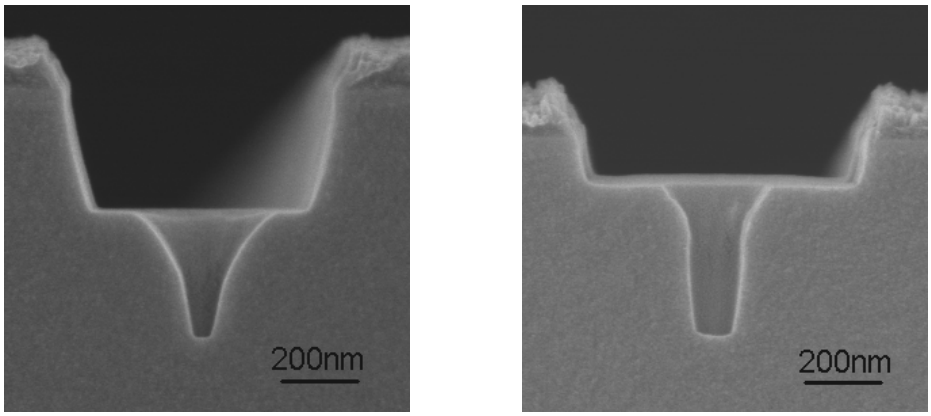


Figure 10.18: Via facet formation in line etch process for multilevel S-FIL

10.6.4 Facet Control in Line Etch

Reducing the RF power of the etching process was first considered as a means to suppress the facet formation. The experiment in Figure 10.8 was repeated with the RF power reduced by nearly 50% (1500W to 800W). The result is shown in Figure 10.19 (a) and clearly indicates that reducing the RF power did not effectively suppress the via facet formation. However, it was observed that the via faceting was less significant when the etching process was intentionally terminated early in time (~1/3 etch time), as shown in Figure 10.19 (b). Due to the reduced etching time, the line height is about 1/3 of the intended final height but the faceting is greatly reduced.

The implication of this finding is that the via facet is not a steady state characteristic of the C_4F_8 chemistry. The facet develops over the etch time instead of forming immediately when exposed to the etch chemistry. This observation opens doors to optimization of line etch based on C_4F_8 chemistry that generates vertical sidewall but produces via faceting.



(a) (b)

Figure 10.19: 120 nm via structure after line etch using C_4F_8 chemistry (a) at reduced RF power and (b) for a reduced etch time – SEM courtesy of SVTC, Inc.

10.7 FACET FORMATION

10.7.1 Hypothesis

As discussed earlier, reducing RF power did not show any significant alleviation of the facet problem, and the via faceting increases over the course of the line etch. Based on these observations, a hypothesis was made that the rate of facet formation has the following functional form.

$$F = f(\rho), \text{ where} \tag{10.2}$$

$$\rho = \frac{R_s}{R_{chem} + R_s} \tag{10.3}$$

where F is the rate of facet formation, R_s is the etch rate due to physical sputtering, R_{chem} is the rate of chemical etching, and ρ is the ratio of physical etching rate to the overall etching rate. This hypothesis specifies that via faceting increases at certain rate F, as suggested by the result of Figure 10.19. Reducing the RF power lowers the sputtering rate, but it also lowers the chemical etching rate. The result is that the ratio ρ and therefore the faceting remain relatively unchanged despite the reduction in RF power.

Based upon this hypothesis, reduction of facet formation can be achieved by reducing ρ, the ratio of physical etching rate to overall etching rate. Obviously to reduce this ratio, one can either choose to decrease the numerator (physical etching rate), or increase the denominator (overall etching rate). The experiment shown in Figure 10.19 (b) was designed to achieve the former. Clearly, it was unsuccessful. This is because the overall etching rate was lowered at the same time. It is known that ion bombardment enhances the chemical etching rate of the fluorinated SiO_2 surface in

fluorocarbon plasma [10.8,10.9]. The complex surface mechanism involved in plasma etching was reviewed by Oehrlein *et al*. [10.10]. The other way to lower the ratio ρ is to increase the overall etching rate while keeping the physical etching rate constant. This can be achieved by adding CF_4 to the C_4F_8 chemistry. Jiang *et al*. [10.11] indicated that by doing so, the etching rate increases substantially with only minimal effect on the final pattern profile.

It is critical to point out that the hypothesis described by Equation (10.2) is only taken to facilitate the development of this line etch process. A detailed mechanistic understanding of the etching reaction is not within the scope of this study.

10.7.2 Objective

In order to develop an RIE process in which the etching rate is increased without a substantial increase in the physical bombardment rate, a design of experiments was performed to explore the etching rate of CF_4/C_4F_8 chemistry at a constant RF power. This design used the process that produced the result in Figure 10.19 as the baseline. The etching rate of the low-k ILD was approximately 1750 Å/minute with this baseline process. The goal of the experiments was to find a ratio of CF_4/C_4F_8 in which, under the same RF power, the chemistry gives an approximate etching rate three times the baseline process, or above 5250 Å/minute.

10.7.3 Experimental

Objective

Low-k ILD etch rate ≥ 5250 Å/minute

Factors

C_4F_8: $25\% > C_4F_8 > 2.5\%$

CF_4: $75\% > CF_4 > 5\%$

Diluent gas: $80\% > Ar+N_2 > 20\%$ (N_2:Ar=3:2)

Composition of component gas was determined by gas-feed flow rates.

Response

Low-k ILD (Black Diamond®) etch rate

Constants

Power:	800 W
Pressure:	50 mT
Substrate temperature:	60 °C

Figure 10.20 shows a ternary plot for the design of experiments for CF_4/C_4F_8 chemistry. A total of 17 experiments were conducted. Fourteen of them, labeled in blue points in the plot, were the original design of experiments, which included the extreme and middle points on the variable limits and variable space, as well as the quarter points along the CF_4 range. However, the objective etch rate was not achieved in the original design of experiments. Therefore, three additional experiments, labeled in red

points, were conducted based on the trend observed in the original design of experiments. The following discussion reports the analysis based on the results of all 17 experiments.

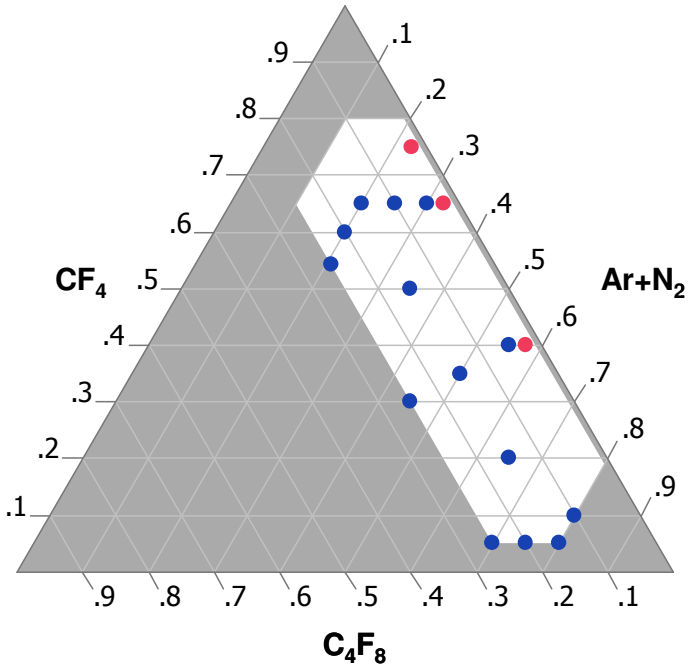


Figure 10.20: Ternary plot of the variable factors in the design of experiments of etching chemistry based on CF_4/C_4F_8 mixture (the blue points are the original experiments and the red points are the additional experiments)

These experiments were conducted on the wafers coated with a 1 μm thick blanket film of low k dielectric Black Diamond®. Ellipsometric measurement of the film thickness was conducted at 17 concentric locations on the wafers before the etch experiment, as shown in Figure 10.21. During the etch experiments, each wafer was subjected to one etching condition for 1 minute. The thickness at the same locations was measured with the ellipsometer after etch. The etch rate was calculated from the difference of the two measurements divided by the etch time.

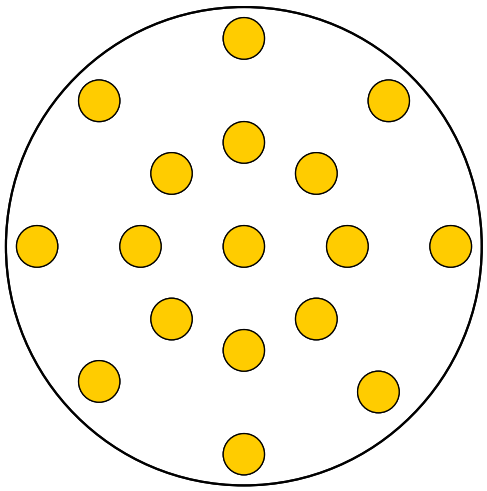


Figure 10.21: Ellipsometer measurement location on a wafer

It is interesting to note that there is one missing point at the bottom right corner of the factor space (low C_4F_8 and high diluent gas). This condition was originally included in the design of experiments. However, it was discovered that the amount of ILD film etched with such process could not be measured with the ellipsometer using known ILD optical properties. This result was reproducible when the experiment was repeated. It is well known that fluorocarbon film growth rather than etching occurs in fluorine-deficient, fluorocarbon high density plasma without substrate bias [10.12]. Therefore, it is a reasonable deduction that thick fluorocarbon polymer film deposition under this condition resulted in the poor ellipsometer measurements of this data point. If this was the case, the additional surface layer altered the optical properties of the stack and therefore the ILD thickness could no longer be measured based on the original assumptions about optical properties. We did not obtain further experimental evidence to support this deduction because the objective etch rate was achieved under other conditions and therefore these data points were not critical in our experiment.

10.7.4 Results and Discussion

10.7.4.1 Etch Rate

Figure 10.22 shows that the ILD etch rate increases with the increase of CF_4 proportion in the mixture. In this figure, the proportion of C_4F_8 was kept constant (C_4F_8 = 0.15). Because the proportions of the ingredients sum to 1 in the mixture, the diluent gas (Ar/N_2) proportion decreased with increasing CF_4 proportion.

In order to determine the condition under which the objective ILD etch rate is achieved, the effects of both CF_4 and C_4F_8 were considered. The experimental results were analyzed with JMP® 6 using an effect screening model by least squares. Figure 10.23 (a) shows the predicted contour plot of the ILD etch rate with respect to CF_4 and C_4F_8 proportions. Figure 10.23 (b) shows the actual by predicted plot that indicates the correlation between experiment data and the model predictions. The red dotted lines show the confidence interval of the model prediction.

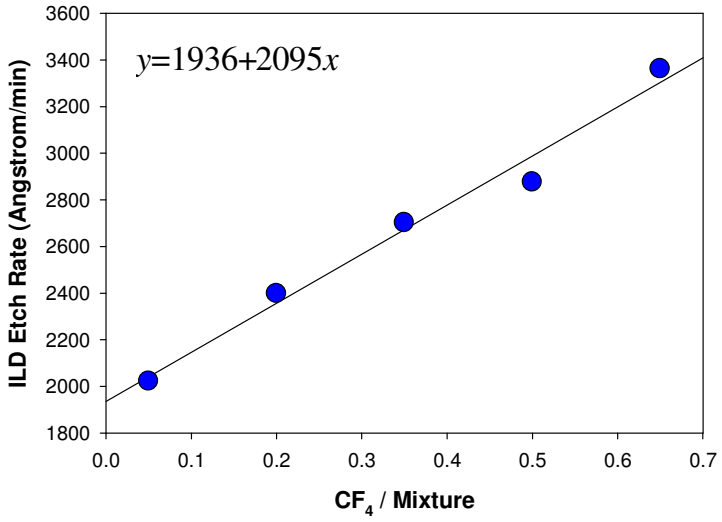
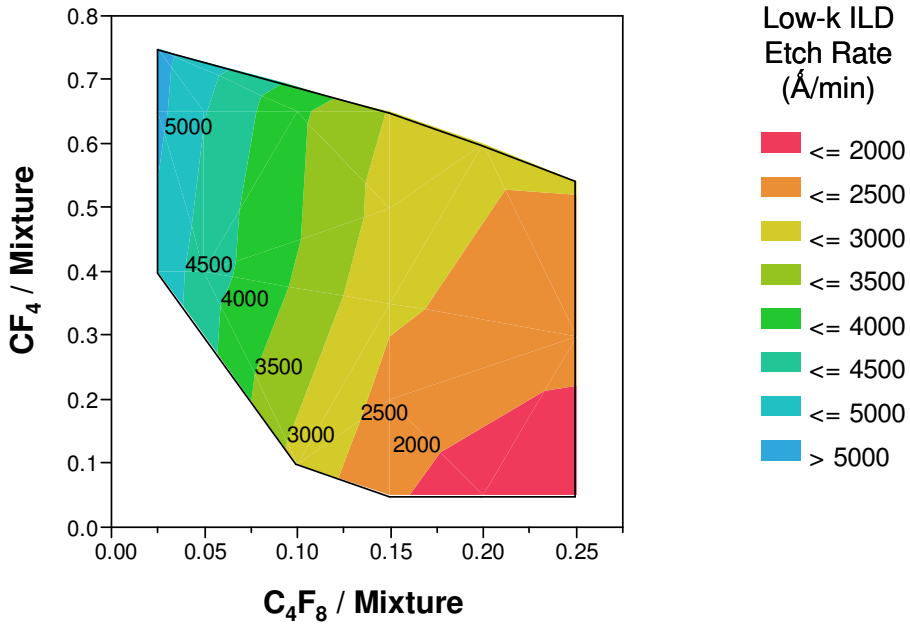
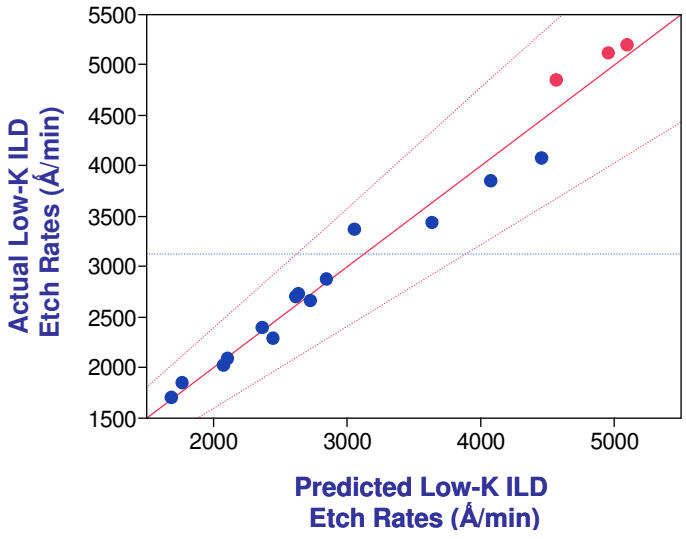


Figure 10.22: ILD etch rate with respect to CF_4/mixture ratio (C_4F_8/mixture is constant 0.15)



(a)



(b)

Figure 10.23: Low-k ILD etch rate: (a) predicted contour plot with respect to proportions of CF_4 and C_4F_8 to the three-component mixture of $CF_4/C_4F_8/(Ar+N_2)$, and (b) the actual by prediction plot (the blue points are the original experiments and the red points are the additional experiments)

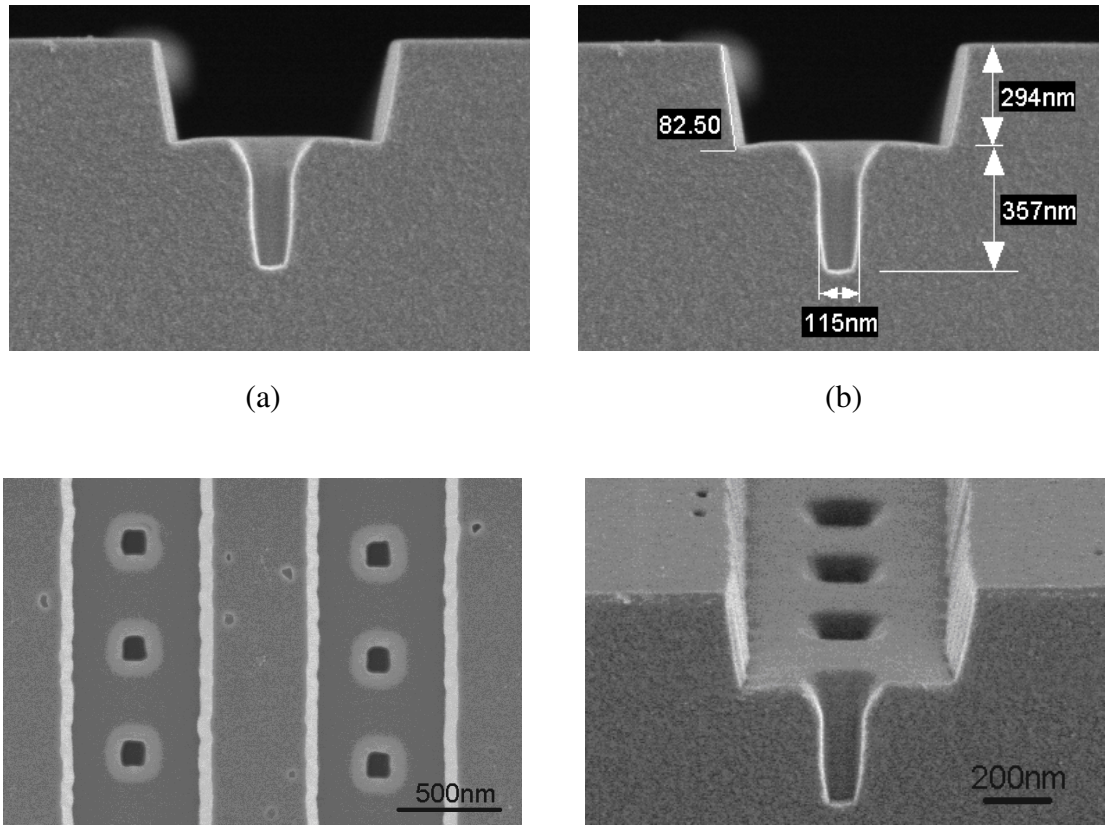
According to Figure 10.23, the low-k ILD etch rate increases as the C_4F_8 proportion decreases and as the CF_4 proportion increases. The maximum ILD etch rate observed in this experiment was 5198 Å/minute under the condition, C_4F_8 = 0.025 and CF_4 = 0.75. However, this requires very low flow rate of Ar, which is close to the lowest Ar flow rate allowed on the plasma etcher. Therefore, the condition C_4F_8 = 0.025 and CF_4 = 0.5 was chosen instead because it has high etch rate (~5000 Å/minute) and all gas flows are stable.

10.7.4.2 Etch Profile

The recipe developed above was used in the line etch of the multistep etch scheme for multilevel dual damascene imprint features. Two standard low-k dielectrics were used in separate experiments. The etch profile of the first ILD material, Black Diamond® is shown in Figure 10.24. The results of the second ILD material, CORAL® are shown in Figure 10.25 and Figure 10.26.

In Figure 10.24, the via bottom did not stop on any additional layer of material because the ILD layer thickness is greater than the feature height. Some defects are visible at the top of the line level. They were caused by slight over etching at the line descum step and the process has been subsequently optimized so that such defects do not occur.

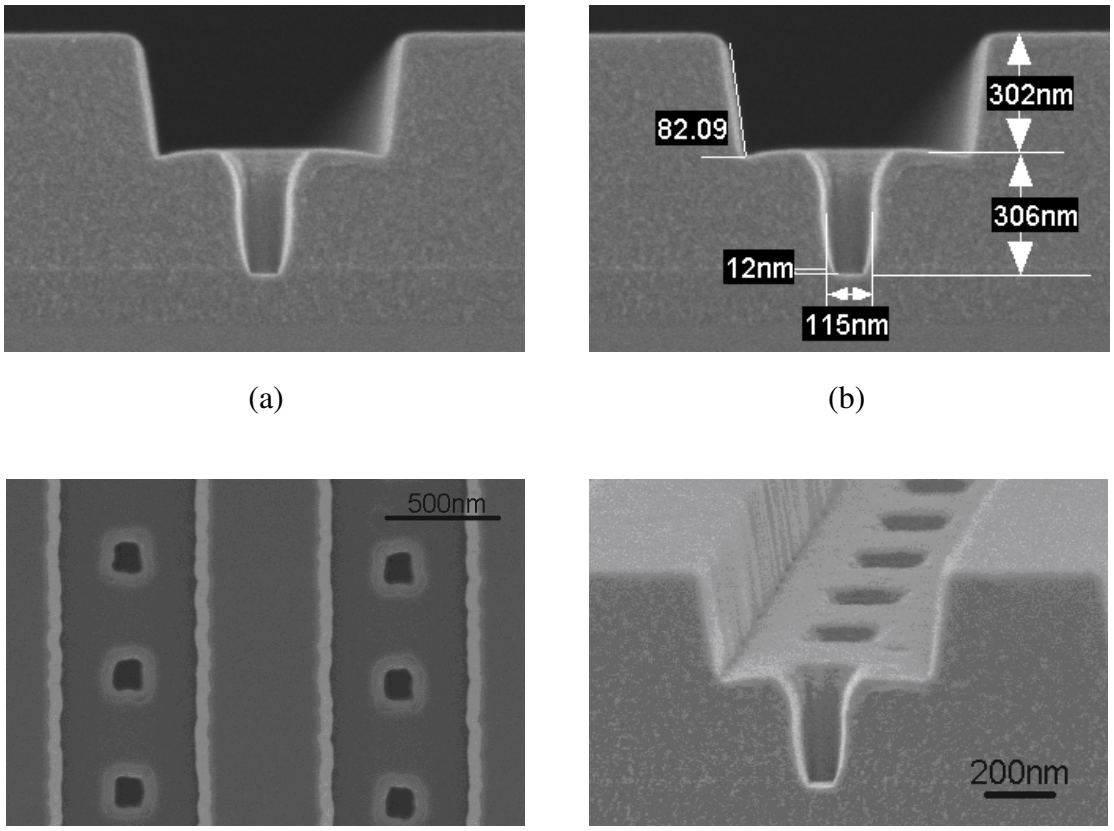
Figure 10.25 shows the etch profile of the nominal 120 nm via structure demonstrated on a 610 nm thick low-k ILD CORAL® layer over a 250 nm SiCN layer. The via was etched approximately 12 nm into the underlying SiCN layer. The via height is therefore reduced because the etch rate of SiCN is approximately six times lower than that of the low-k ILD.



(a) (b)

(c) (d)

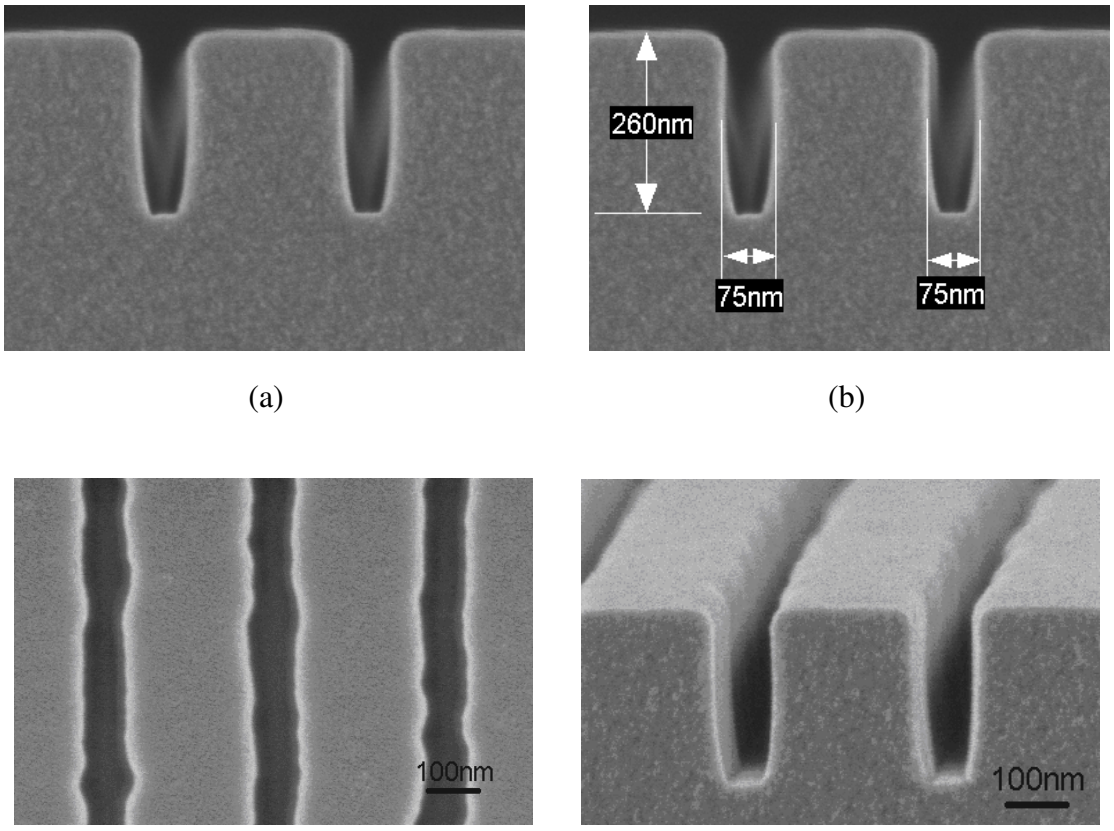
Figure 10.24: Etch profile of dual damascene feature of nominal 120 nm via on low-k ILD 1 (Black Diamond®): (a) cross section SEM, (b) cross section SEM with metrology, (c) top-down SEM, and (d) tilt-shot SEM – SEM courtesy of SVTC, Inc.



(a) (b)

(c) (d)

Figure 10.25: Etch profile of dual damascene feature of nominal 120 nm via on low-k ILD 2 (CORAL®): (a) cross section SEM, (b) cross section SEM with metrology, (c) top-down SEM, and (d) tilt-shot SEM – SEM courtesy of SVTC, Inc.



(a) (b)

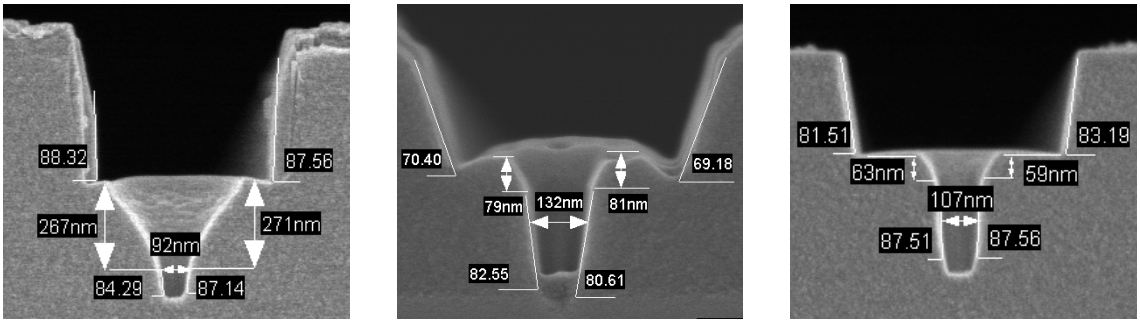
(c) (d)

Figure 10.26: Etch profile of dense lines feature of nominal 125 nm lines with 175 nm spacing on low-k ILD 2 (CORAL®): (a) cross section SEM, (b) cross section SEM with metrology, (c) top-down SEM, and (d) tilt-shot SEM – SEM courtesy of SVTC, Inc.

Figure 10.26 shows the etch profile of nominal 125 nm lines with 175 nm spacing. The etched features show a final width of 75 nm as measured at the mid-height of the line structure in the cross section SEM image. The CD shrink is due to the etch process and will be discussed further in Chapter 11. Line edge roughness (LER) analysis was conducted on the top-down SEM images of the dense lines using SuMMIT software (SEM Metrology Interactive Toolbox) V.6.1.0 by EUV Technology. The results showed that these lines are 71.9 nm in mean CD, 11.55 nm in LER, and 16.75 nm in line width roughness (LWR). The LER is nearly 16% of the line CD and is excessive. However, these lines were shrunk from a nominal 125 nm CD on the template. Therefore, the LER is actually 9.25% of the template CD. This value appears more acceptable but still requires improvement. ITRS specifies the requirement for LER to be less than 8% of the CD [10.13]. However, this requirement is imposed on the lithographic process, not the etch process.

10.7.4.3 Etch Profile Metrics

Based on the results demonstrated in Figure 10.24 through Figure 10.26, the via faceting issue was successfully solved by the etch process developed from the design of experiments. Comparison was made between etch profiles made by C_4F_8, CF_4, and C_4F_8/CF_4 chemistries in order to evaluate the via facet suppression achieved. Five profile related quantitative and qualitative metrics were used for comparison: via facet (quantitative), via sidewall angle (quantitative), line sidewall angle (quantitative), micro-trenching (qualitative), and line bottom smoothness (qualitative). The metrology is shown in Figure 10.27. The via facet was characterized as the vertical distance between top and bottom corners of the ~45° slant at via entrance. The angles of both via and line sidewalls were measured. Micro-trenching and line roughness were also compared.



(a) (b) (c)

Figure 10.27: Etch profile of nominal 120 nm dual damascene feature using: (a) C_4F_8 chemistry, (b) CF_4 chemistry, and (c) C_4F_8/CF_4 chemistry – SEM courtesy of SVTC, Inc.

The profile metrics measured for different line etch chemistries are listed in Table 10.1. The best performer in each metric is marked in bold face font, and the unacceptable performers are marked in italic face font. C_4F_8/CF_4 chemistry clearly renders superior feature profiles in most of the quantitative and qualitative metrics of the etch profile. It outstrips the other two processes in the most critical metrics, that is, vertical via sidewall and low via faceting. The only category in which it did not excel among the three versions was the line sidewall angle. It is not unexpected because the strategy to suppress via faceting was to increase the chemical etching rate. However, the line sidewall is still well within an acceptable range.

Table 10.1 Profile metrics of via features etched with different chemistries

Metrics	C_4F_8	CF_4	C_4F_8/CF_4
Via Facet (nm)	*269*	80	**61**
Via Sidewall Angle (°)	85.8	81.6	**87.5**
Line Sidewall Angle (°)	**87.9**	69.8	82.4
Micro-trenching	**No**	*Yes*	**No**
Line Bottom Surface	**Smooth**	*Rough*	**Smooth**

10.8 OPTIMUM MULTI-STEP ETCH SCHEME

10.8.1 Chemistry

Table 10.2 reports the recipes of the optimized etch process. Table 10.3 shows the etch characteristics of the optimized recipes for the multi-step etch scheme of the pattern transfer for dual damascene multilevel S-FIL.

Table 10.2: Optimized recipes for multi-step etch scheme

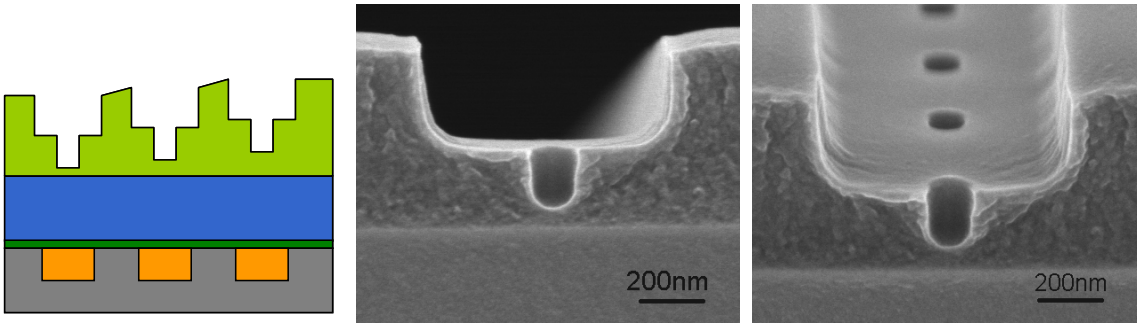
Etch Step	Pressure (mT)	Power (W)	Etch Gases (% total flow rate)			
Residual Open	40	500	80% N_2	20% H_2		
Via Etch	75	1500	0.7% C_4F_8	79.6 Ar	19.7% N_2	
Line Descum	40	500	80% N_2	20% H_2		
Line Etch	50	800	2.5% C_4F_8	50% CF_4	19% Ar	28.5% N_2
Ash	40	500	80% N_2	20% H_2		

Table 10.3: Multi-step etch scheme and etch chemistries

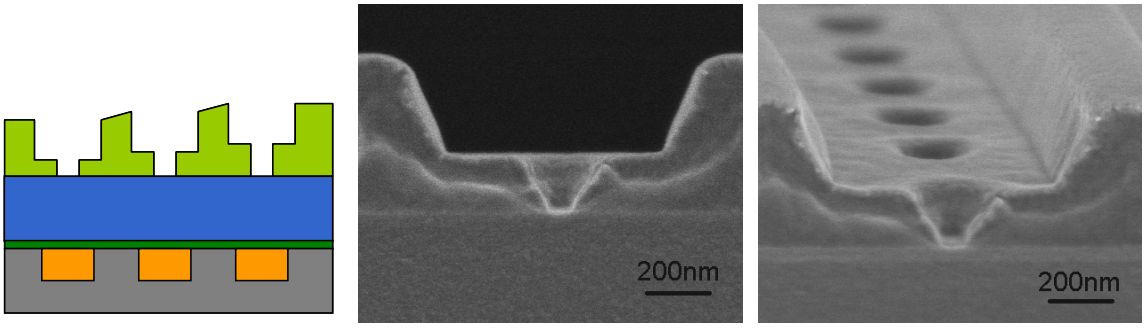
Etch step		**Residual open**	**Via etch**	**Line descum**	**Line etch**	**Ash**
Chemistry		H_2/N_2	C_4F_8	H_2/N_2	C_4F_8/CF_4	H_2/N_2
Etch type		Time	Time	End-point	Time	End-point
Etch Rate (Å/min)	**ILD**	60	2640	60	4980	60
	Resist	2280	840	2280	2400	2280
Selectivity (ILD/R)		1/38	3.1	1/38	2.1	1/38

10.8.2 Experimental Results

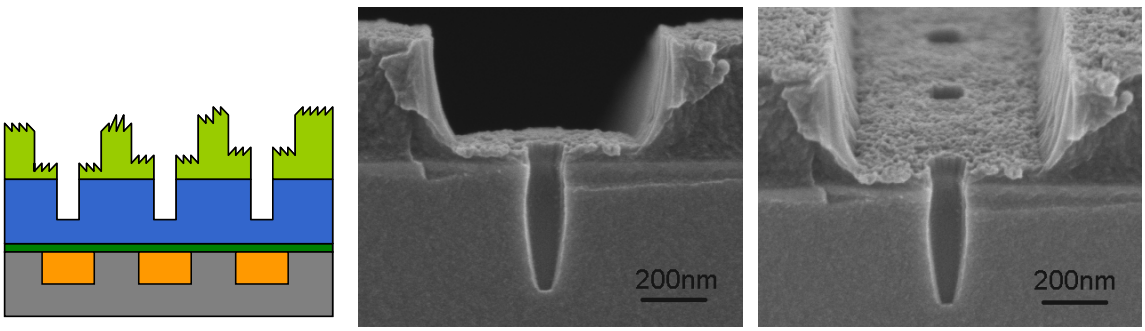
Figure 10.28 shows the experimental results of each step of the multi-step etch scheme of a nominal 120 nm dual damascene structure made with multilevel S-FIL. The results indicate that the optimized multi-step etch scheme provides faithful pattern transfer capability for the dual damascene patterns imaged with multilevel Step and Flash Imprint Lithography. Further evaluation of the performance of the etch process is given in Chapter 11.



(a)

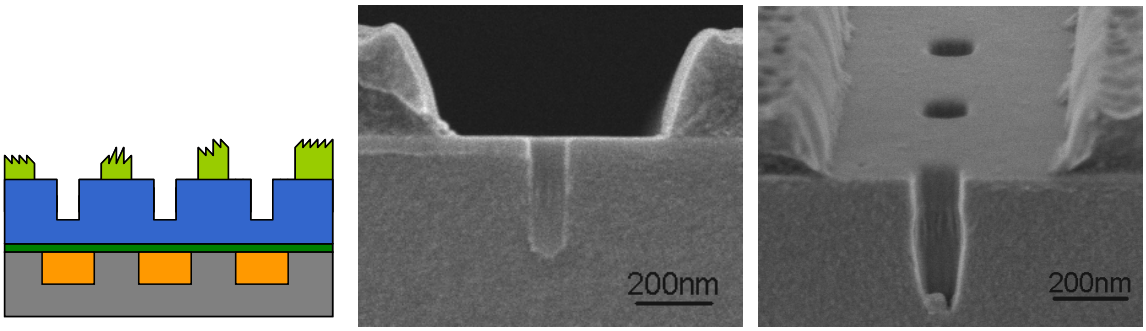


(b)

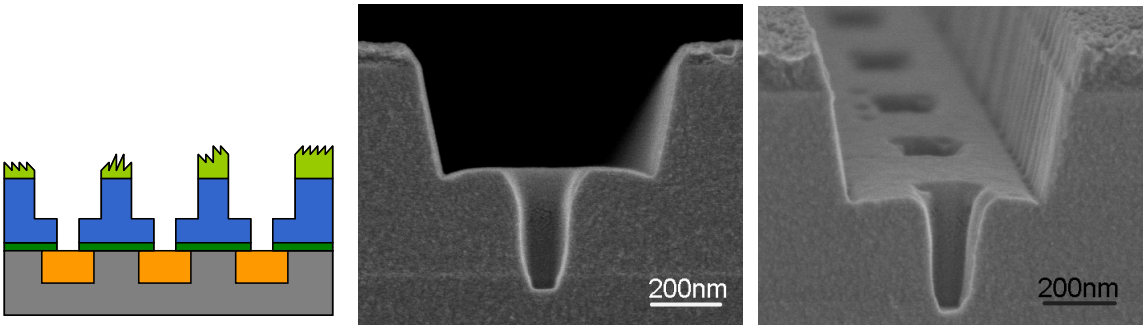


(c)

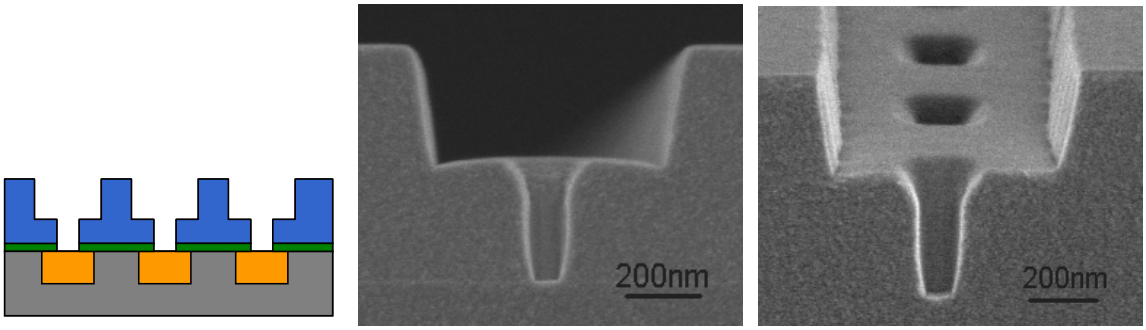
Figure 10.28: Optimized pattern transfer of 120 nm dual damascene structure using multi-step etch scheme and multilevel Step and Flash Imprint Lithography: (a) imprint, (b) residual open, (c) via etch, (d) line descum, (e) line etch, and (f) ash; *figure continued in next page* – SEM courtesy of SVTC, Inc.



(d)



(e)



(f)

Figure 10.28: Optimized pattern transfer of 120 nm dual damascene structure using multi-step etch scheme and multilevel Step and Flash Imprint Lithography: (a) imprint, (b) residual open, (c) via etch, (d) line descum, (e) line etch, and (f) ash; *figure continued from previous page* – SEM courtesy of SVTC, Inc.

10.9 CONCLUSIONS

The development of a pattern transferring etch process for multilevel Step and Flash Imprint Lithography was described in this chapter. The challenges in the pattern transfer of multilevel patterns were identified and solved. We proposed a multi-step etch scheme and conducted path finding experiments to identify the desired chemistry for each etching step. The line etch step was found to be the most challenging due to excessive via faceting. A design of experiments was conducted to optimize the line etch chemistry based on a C_4F_8/CF_4 mixture. Satisfactory etch profiles were obtained using the multi-step etch scheme.

The most important advantage of the multistep etch scheme is its capability of faithful pattern transfer with minimal etch artifacts such as via faceting or line bottom roughness. This capability was demonstrated with the etching chemistry and a tool set which is currently used in industry for BEOL dielectric etching. It is also based on a commercially available imprint resist. Therefore, there are no known barriers for the insertion to this technology into the existing processing flow.

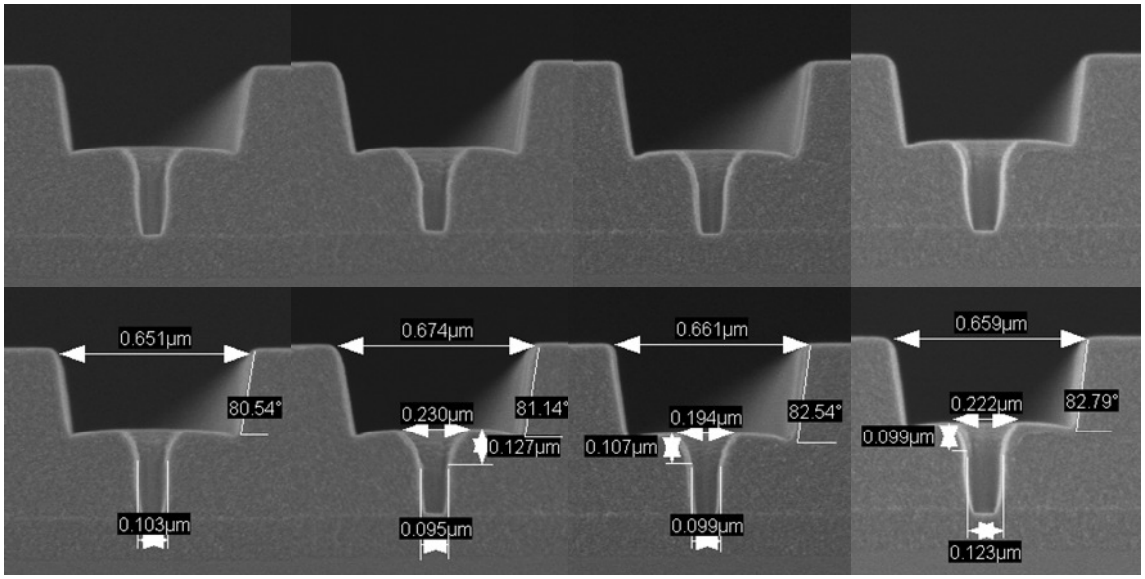
Chapter 11: Pattern Transfer II – Process Evaluation

11.1 INTRODUCTION

Chapter 10 described the development of an *in-situ* multistep etch scheme that enables faithful pattern transfer of the multilevel imprints and meets the etching challenges of etch artifacts, via faceting and imprint non-uniformity. This chapter examines the important characteristics of the multistep etch scheme, including its process window and line edge roughness. This chapter also reports an RIE controlled CD shrink technique that was discovered during the etch experiment.

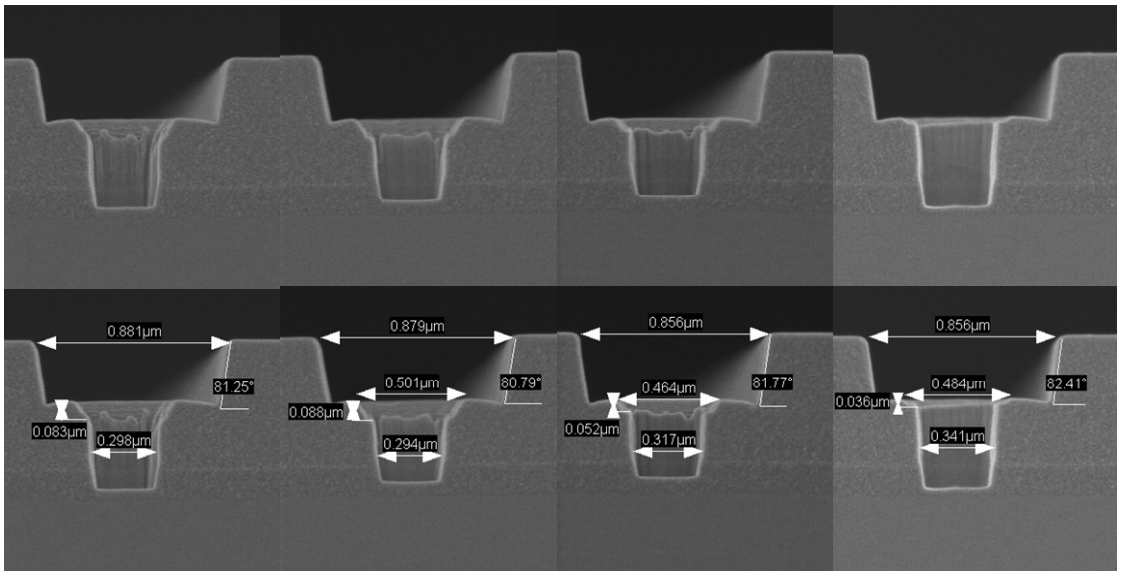
11.2 PROCESS WINDOW

The process window was defined as the allowed variation in process conditions with which the desired final feature can be obtained. Figures 11.1 through 11.3 show the etch profiles of features obtained with various line etch conditions. The line etch chemistry was identical for these experiment but the chamber pressure and RF power were varied across wide ranges. The images obtained from these experiments are almost identical. This observation strongly supports our previous hypothesis that the ratio of the etching gas mixture is the key parameter to the final profile rather than the RF power. More importantly, it indicates the breadth of the line etch process window.



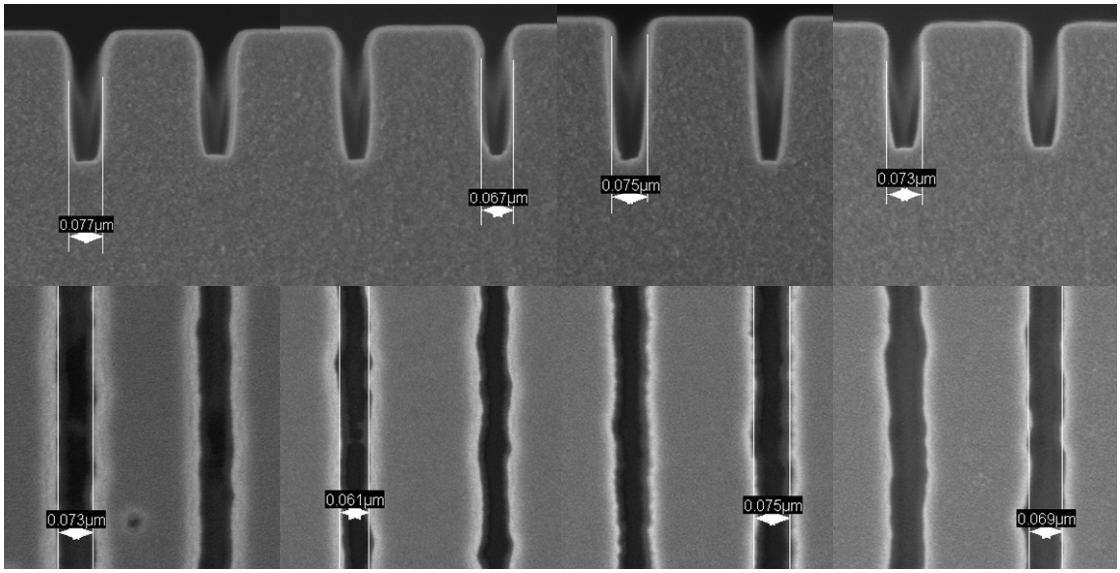
(a) (b) (c) (d)

Figure 11.1: Dual damascene features for 120 nm vias using various line etch: (a) 5mT/300W, (b) 80mT/700W (c) 45mT/700W, and (d) 75mT/400W – SEM courtesy of SVTC, Inc.



(a) (b) (c) (d)

Figure 11.2: Dual damascene features for 350 nm vias using various line etch: (a) 45mT/300W, (b) 80mT/700W (c) 45mT/700W, and (d) 75mT/400W – SEM courtesy of SVTC, Inc.



(a) (b) (c) (d)

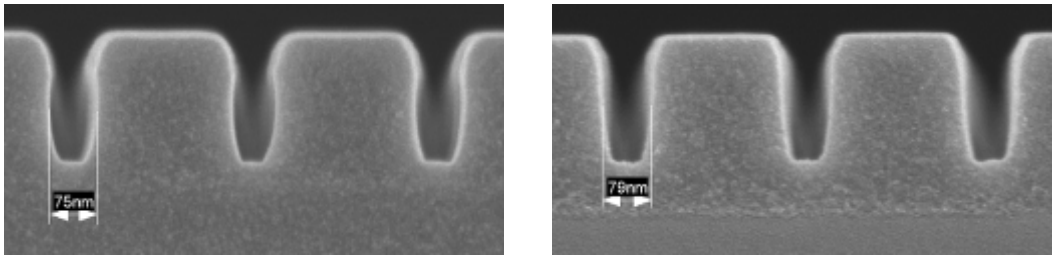
Figure 11.3: 125 nm / 175 nm dense lines using various line etch: (a) 45mT/300W, (b) 80mT/700W (c) 45mT/700W, and (d) 75mT/400W – SEM courtesy of SVTC, Inc.

In Figures 11.1 through 11.3, there was modest variance in feature CD. We could not prove whether this small variance resulted from the etch process or from the template CD variance unless we carry out destructive tests on the rare and expensive template or run large numbers of repeated experiments which is also very expensive and beyond the scope of this study. The results in this section show that the multi-step etch scheme exhibits a wide process required for a commercially feasible etch process for the BEOL technology using multilevel Step and Flash Imprint Lithography.

One minor concern could be raised regarding the etch profiles of dense lines shown in Figure 11.3 (a), (b), and (d). These cross sectional images show some degree of necking at the top of the lines. Necking could cause Cu filling issues in subsequent metallization processes. We have found that a mild dilute hydrogen fluoride wet etch

process can solve the necking issue without compromising the critical dimension of these dense lines.

Figure 11.4 (a) shows dense lines with necking. Figure 11.4 (b) shows the dense lines obtained from the identical RIE process followed by a dilute HF wet etch. The necking was substantially reduced with only minimal increase in the line CD. Therefore, this mild wet etch treatment further increases the process window of the line etch process. This wet etch step was therefore introduced to the process flow that produced the wafers for electrical testing.

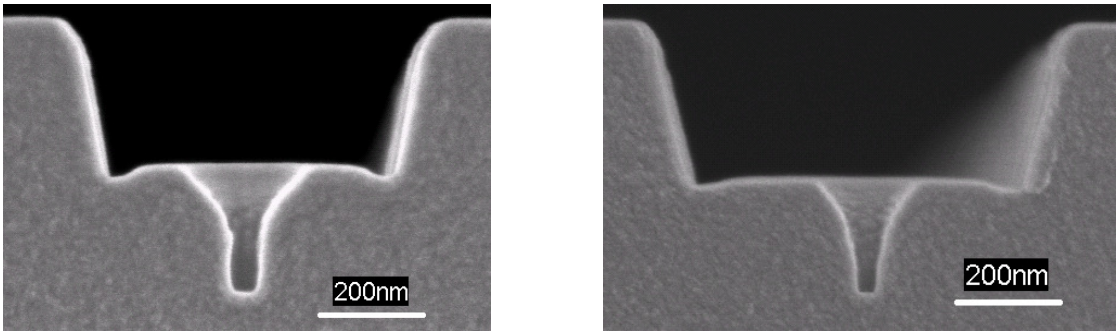


(a) (b)

Figure 11.4: Line necking: (a) before HF treatment, and (b) after HF treatment (HF solution HF:DI water = 1:50) – SEM courtesy of SVTC, Inc.

11.3 RIE CONTROLLED SHRINK

While the multi-step etch scheme has proven effective for faithful pattern transfer, it was also found that this technique offers the unique advantage of a controllable CD shrink through adjusting the via etch step. By changing the etch chemistry of the via etch step, the final critical dimension FCD of the via can be deliberately controlled and shrunk. Figure 11.5 shows the images of two experiments in which the via CD was shrunk from 120 nm (nominal) to 55 nm and 38 nm through the chemistry at the via etch step. Further discussion follows and the recipes are reported in Table 11.1.



(a) (b)

Figure 11.5: RIE controlled shrink from 120 nm template CD: (a) 55 nm and (b) 38 nm – SEM courtesy of SVTC, Inc.

Table 11.1: Via etch recipes for RIE controlled CD shrink experiments

Image	Step	Pressure (mT)	RF (W)	Etch Gases (% total flow rate)			FCD (nm)
Figure 11.15 (a)	(1)	40	1400	30% CF_4	60% Ar	10% O_2	55
	(2)	75	1500	0.7% C_4F_8	79.6% Ar	19.7% N_2	
Figure 11.15 (b)	(1)	50	800	2.5% C_4F_8	10% CF_4	87.7% N_2	38

In both CD shrink experiments, only the via etch recipes were changed, while the other etch steps used the optimum recipes reported in Table 10.2. For the experiment in Figure 11.5 (a), the via etch used two chemistries sequentially, a CF_4/O_2 chemistry and then a C_4F_8 chemistry. For the experiment of Figure 11.5 (b), a variation in C_4F_8/CF_4 chemistry was used. It indeed was an interesting discovery and could provide a solution to future extension of the patterning capability of lithographic processes.

11.4 LINE EDGE ROUGHNESS (LER)

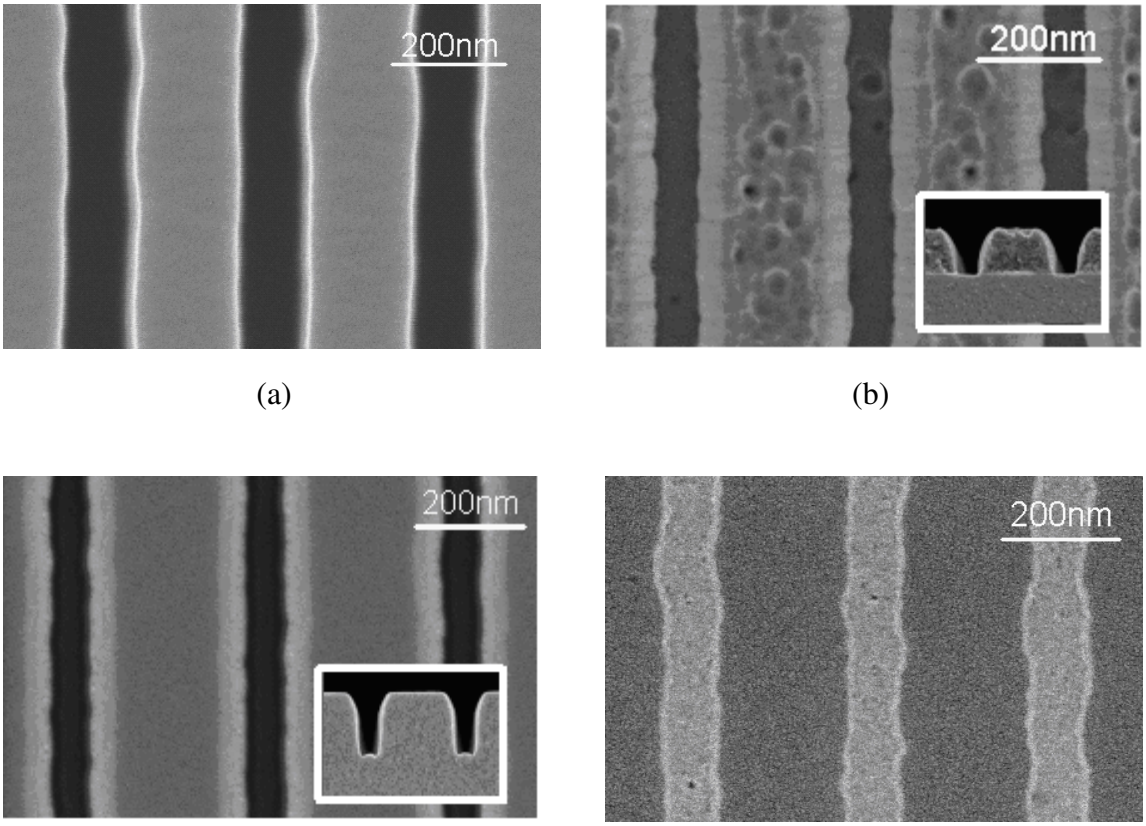
Line edge roughness has been widely recognized as one of the major challenges in continued device scaling. The electrical resistance of a conductor arises from the scattering of the electrons at imperfect sites such as surfaces and boundaries. For Cu, the electron mean free path is about 40 nm at room temperature [11.1]. Hence, the resistivity of Cu increases nearly exponentially with the dimension of the interconnect due to the combined effect of enhanced sidewall scattering and grain boundary scattering in sub 100 nm fine lines [11.2]. Therefore, for interconnect below 50 nm, LER is not only an undesirable process induced artifact, but also an active factor in causing the increase in the size-dependent resistivity [11.3].

For photolithography, LER results from various sources, such as diffusion of acid catalyst, exposure shot noise, etc. For S-FIL, however, feature patterning is accomplished through physical confinement of liquid monomers and therefore is free of the diffusion controlled reactions that can cause excessive LER. In fact, control of line edge roughness in S-FIL resides in the ability to manufacture low LER templates.

The focus of this study was to evaluate multilevel S-FIL so attention was paid to LER throughout the process flow. Unlike the conventional dual damascene process in which the via and the line patterning steps are separate, the S-FIL process requires the line resist to withstand the entire etching process. Before the line level resist is used for pattern transfer, it goes through three etching steps each with different chemistries: residual layer open, via etch, and line descum. The possibility of pattern distortion during such extended etching poses a logical concern and was therefore studied.

Figure 11.6 shows top-down SEM images of the nominal 125 nm dense lines at various steps of the etching process. Figure 11.6 (a) shows line patterns as imprinted. Figure 11.6 (b) shows the patterns after the descum etch is completed. Figure 11.6 (c)

shows the fully etched line patterns with the resist stripped off. Figure 11.6 (d) shows the Cu line patterns after CMP. Each image was taken at 100K magnification and contains 4 line segments about 0.95 μm in length.



(a) (b)

(c) (d)

Figure 11.6: 125 nm / 175 nm dense lines at different step of the etching process – SEM courtesy of SVTC, Inc.

LER/LWR analyses were conducted on these SEM images using SuMMIT 6.1.0 software by EUV technology, Inc. The reported LER is the single-sided 3-sigma edge variation from a straight line. The LWR is a 3-sigma reading of the line-width variation. Both are in accordance with the ITRS definition. Spectral filtering was

applied to eliminate high and low frequency noises. The high frequency threshold is 200 μm^{-1} (period 4 nm), near the resolution of the SEM images taken. The low frequency threshold is 2 μm^{-1} (period 500 nm), near the dimensions of the measured line segments.

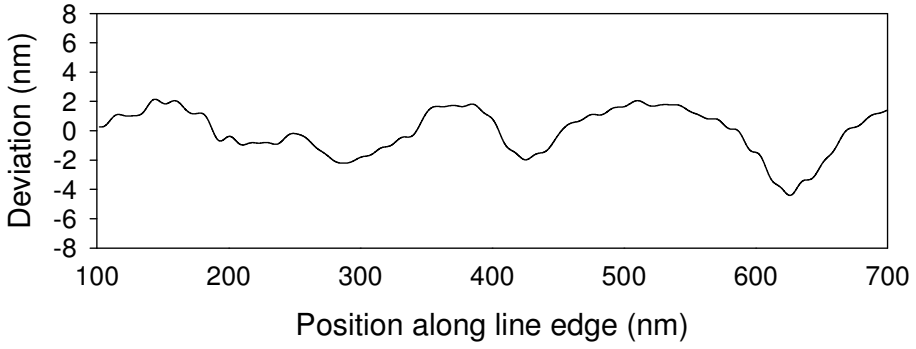
The results of the LER/LWR analysis are listed in Table 11.2. The imprinted lines have 5.9 nm average LER and 9.3 nm average LWR, which very likely results from the template fabrication rather than the imprinting process. In addition to the imprint induced roughness, extended etching steps indeed gradually increased the line roughness. Fortunately, LWR only increased by 7.5% and LER by 18% from the imprint to the fully etched patterns. The final metallized pattern showed an increase of roughness by a larger margin, that is likely to arise from the difference in metrology. Figure 11.6 (a) through (c) are all line patterns with >200 nm topography. Figure 11.6 (d), however, is an image of the Cu lines after the CMP step and therefore the SEM image was taken over only negligible topography.

Table 11.2 Line edge roughness and line width roughness

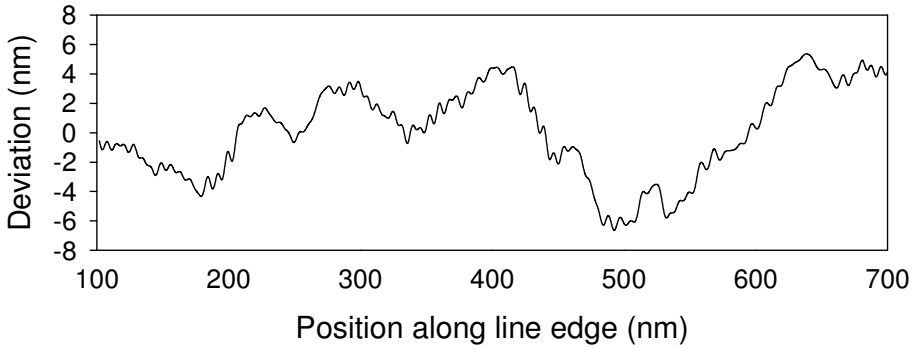
Step	Imprint	Before Line Etch	Etch Complete	Metallized
Figure	Figure 11.6 (a)	Figure 11.6 (b)	Figure 11.6 (c)	Figure 11.6 (d)
CD (nm)	101.9 ± 5.1	78.7 ± 0.9	72.0 ± 1.5	104.2 ± 4.3
LER (nm)	5.9 ± 1.7	7.7 ± 0.6	7.0 ± 2.0	11.1 ± 1.1
LWR (nm)	9.3 ± 2.5	10.1 ± 0.7	10.0 ± 3.4	17.1 ± 3.9

Close observation of these images reveals that the imprinted line pattern, as in Figure 11.6 (a), has very little high frequency roughness compared to the partially etched pattern in Figure 11.6 (b). This difference can be characterized by the line edge plots and the spectral analysis of the line edges. Figure 11.7 shows the line edge plots at the critical process steps: (a) imprint, (b) line descum, and (c) fully etched. All line edges are similar in low frequency variation and amplitude. High frequency small amplitude roughness can also be observed. While the initial imprint only has minimal high frequency roughness, the plot of the partially etched sample shows a significant increase in this kind of roughness. It is therefore a rational deduction that the high frequency roughness arises from the etching process before the clearance of the resist at the line bottom. Nevertheless, the line edge evidently becomes smoother than the intermediate step once the etch process is completed, as shown in Figure 11.7 (c), although still not as smooth as the original imprint.

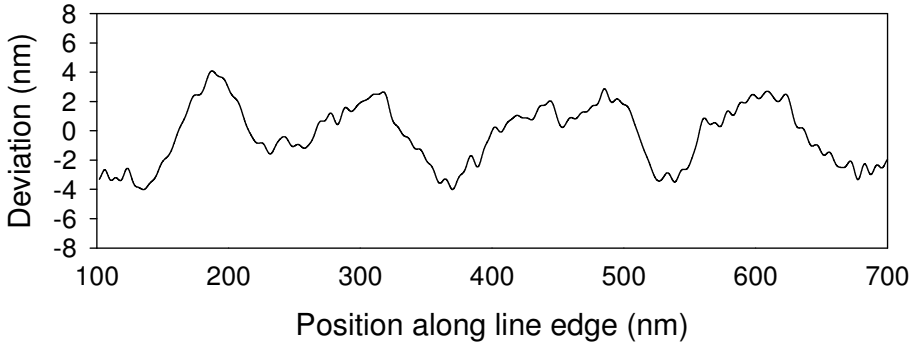
In order to distinguish the high and low frequency roughness, further image analysis was conducted over two spectral ranges: the low frequency region (2 μm^{-1} - 20 μm^{-1}) and the high frequency region (20 μm^{-1} - 200 μm^{-1}). Figure 11.8 shows the LER and LWR derived from these ranges. First, the low frequency roughness is invariably higher than the high frequency roughness. This is an anticipated consequence since low frequency roughness generally has large amplitude and high frequency roughness has small amplitudes. For the three processing steps, the low frequency roughness remains nearly unchanged. The high frequency roughness, however, has very small error bar and shows a clear increase from imprint to line descum.



(a)



(b)



(c)

Figure11.7: Line edge plots at critical process steps: (a) imprint, (b) after line descum, and (c) fully etched. These were not taken at the same place of a line.

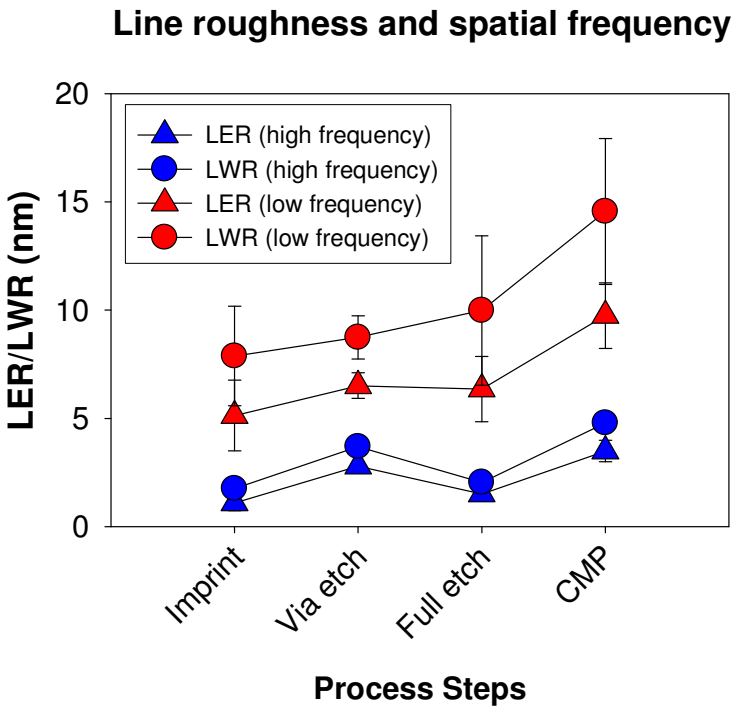


Figure 11.8: Line edge roughness and its spatial frequency at critical processing steps (error bars indicate line to line variation, not intra-line variation)

The implication of the LER results is that the high and low frequency LER may need to be considered separately from both a process and performance point of view. The low frequency large amplitude LER has more pronounced effect on the interconnect linewidth and spacing and this kind of LER is likely to be inherited from the master template rather than the wafer patterning process given the fact that its frequency, amplitude, and LER values remain essentially unchanged through the process. Therefore, improvement will need to be focused on the template fabrication process. Studies showed that resist sensitivity and choice of pattern generator are the keys to improvement of template LER [11.4]. The chief origin of the high frequency low amplitude LER is clearly etch induced because it evolves with the progress of the etch

process. The most possible root cause is resist footing due to the rounded corner of line pattern of the original imprint, as shown in Figure 10.28 (d). Control of the chemical and physical aspect of the etching process as well as its extent is expected to be the key to reducing the high frequency LER.

11.5 ADVANTAGE OF MULTI-STEP ETCH SCHEME

This chapter describes an analysis of the process window of the multi-step etch scheme. The results showed that nearly identical feature profile can still be produced with the optimum etch chemistry when the RF power and the chamber pressure were varied over a significant range. Line edge roughness analysis was conducted for line structures at each critical etch step. The objective was to evaluate the LER increase due to the extended etch process required for the multilevel pattern transfer. The low frequency LER appears to be inherited from the LER on the template and remains constant. The high frequency LER appears to be induced by the etch process. Line edge roughness and its optimization deserve further investigation.

Chapter 12: Yield and Failure Analysis

12.1 INTRODUCTION

This chapter reports the electrical yield of the Back End Of the Line (BEOL) via chain test vehicle using multi-level Step and Flash Imprint Lithography (S-FIL) as the imaging process. The result demonstrates that this new processing technique can provide a high yield solution to the fabrication of BEOL interconnects. Failures encountered in the test vehicle were studied and correlated with the electrical test results. New test structures that were designed to investigate failure modes characteristic to processing using S-FIL were proposed.

12.2 EXPERIMENT

The Metal 1 processing was based on a standard process in SVTC, Austin TX. The Metal 2 level imaging was conducted with multi-level S-FIL, the pattern transfer etch is described in Chapter 10.

12.2.1 Metal 1 Preparation

The dielectric material used in Metal 1 was thermally deposited SiO_2. Metal 1 contains only line structures and was patterned with 248 nm photolithography with 250 nm critical dimension (CD) and the standard M1 line etching process. The Ta barrier and Cu seed layer were deposited with a Novellus Inova PVD system. Electroplating was conducted with a Novellus standard ECP (electrochemical plating) system. The excessive Cu was removed with an Applied Materials CMP (chemical mechanical polishing) system. The last step in M1 processing was deposition of a 60Å SiCN cap

layer, which serves as the inter-level diffusion barrier and prevents Metal 1 Cu from oxidization prior to Metal 2 processing.

12.2.2 Metal 2 Inter-Level Dielectrics

The Metal 2 ILD used in this project was Novellus CORAL® which is a low dielectric constant organo-silicate glass (OSG). The dielectric constant of the blanket ILD film is approximately 2.85. It was deposited in a commercial chemical vapor deposition (CVD) system.

12.2.3 Adhesion Layer

A 125Å thick oxide layer was deposited over the M1 barrier layer with a thermal TEOS (tetra-ethoxy-silane) process. Oxygen plasma treatment was applied before coating the adhesion layer AP410. This treatment was found to provide excellent adhesion between the imprint resist and the low-k ILD.

12.2.4 Imprint

A multilevel S-FIL process was used to generate the imprint pattern. The S-FIL process detail is described in Chapter 9. The template was built to our design by Toppan Photomasks, Inc.

12.2.5 Etch

The multi-step etch scheme used in this study is described in Chapter 10.

12.2.6 Barrier/Seed Deposition

A 175Å Ta barrier and a 700Å Cu seed layer were deposited with a Novellus Inova PVD system.

12.2.7 Cu Electroplating

Electroplating was conducted with a Novellus standard ECP (electrochemical plating) system.

12.2.8 Cu Anneal

After electroplating, the wafer was annealed at 150 °C for 30 minutes to stabilize the Cu grains in order to achieve a consistent polishing rate in the subsequent Cu CMP process.

12.2.9 Cu Chemical Mechanical Polishing (CMP)

The main Cu polishing included three steps. Bulk Cu polishing removed the thick Cu layer over the patterns, and a soft-landing step that utilized a low down-force achieved a low polishing rate to prevent excessive polishing toward the end of Cu polishing. A brief over-polishing step was added to ensure complete removal of the Cu layer. The slurry used in the main Cu polishing steps was Fujimi DCM-CX4.

After the main Cu polishing, a residual Cu CMP step was used to ensure that there was no remaining Cu trace on the polished wafer surface. The slurry used in this step was Cabot 7092.

The Barrier CMP step removed the Ta barrier and exposed the M2 ILD. The slurry for this step was Arch Cu-10K-2

12.2.10 Electrical Testing

The electrical testing was conducted with an HP 4073A in-line parametric tester with a fully automated prober and a 2×12 probe card.

12.3 VIA CHAIN YIELD ANALYSIS

The via chain yield was determined according to the cumulative density function of the via resistance, which was calculated by dividing the measured chain resistance by the number of connected vias (contacts). In this study, vias of a host of design sizes were incorporated into the template. The via resistance varies with the via sizes and, as a result, so does the yield criterion. Figure 12.1 describes the yield criteria in this study, which are 50% above and below the mean of the main data distribution.

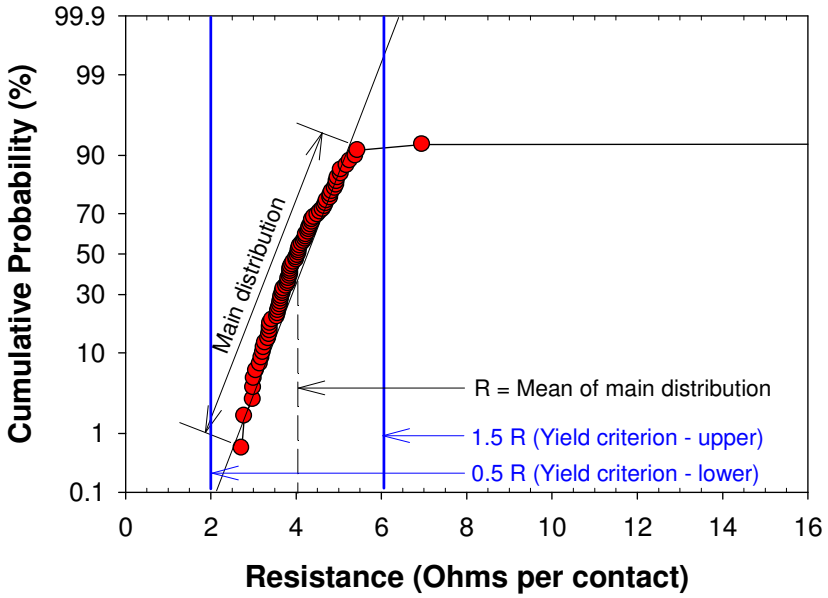


Figure 12.1: Determination of via chain yield

All test structures have 8 identical repetitions on the template. Thirty seven die were printed and 21 of them, excluding the edge die, were tested on each wafer, as reported in Section 9.6. Yield of two processes are reported: the process with optimum feature profile (Section 12.3.1) and the process with optimum yield (Section 12.3.2).

12.3.1 Process Version I: Optimum Feature Profile

12.3.1.1 Feature Profile

Figure 12.2 shows the pre-CMP SEM image of the dual damascene feature using the optimum etch process reported in Table 10.2. The via generated with this process from the 120 nm nominal template CD was 115 nm as measured at the mid point of the via height. The final via height was 272 nm, which was higher than the 240 nm via height on the master template. The effective via aspect ratio of the Cu via was close to 2.4, which considerably exceeds the ITRS Metal 1 aspect ratio requirement of 1.7 for 90 nm node [12.1]. After the metallization processes were completed, the electrical conductivity of the via chains was tested .

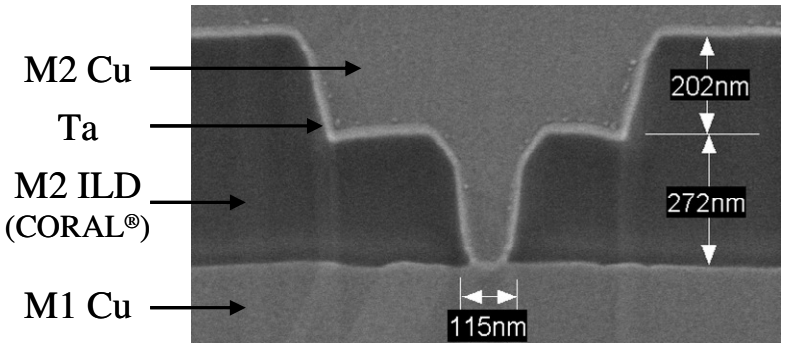


Figure 12.2: Pre-CMP dual damascene feature of nominal 120 nm via. Final via CD is 115 nm measured at the mid point of via height – SEM courtesy of SVTC, Inc.

12.3.1.2 Kelvin Vias

Kelvin vias are the single contact via structures used for basic qualification of the BEOL process. Figure 12.3 (a) shows the cumulative density function (CDF) of the Kelvin via resistance of the dual damascene structures. The yield of the Kelvin via reached 96% for the 120 nm vias and higher for the larger structures. The conductivity of the Kelvin via test structures confirmed that multilevel S-FIL can successfully connect the via and the line of the Metal 2 level to Metal 1. However, advanced BEOL imposes very stringent demands on the interconnect yield and this can best be investigated with the multiple-contact via chains.

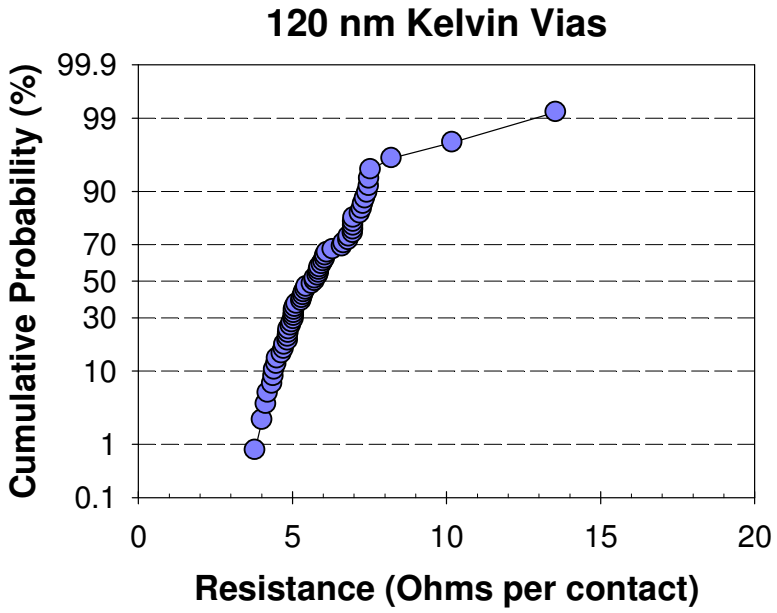


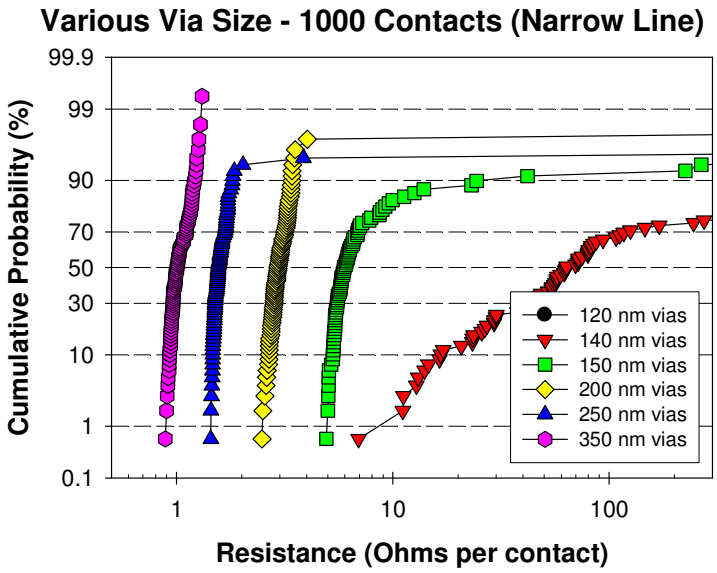
Figure 12.3: Via resistance of 120 nm Kelvin vias (Via sizes specified are nominal via sizes on the template)

12.3.1.3 Via Chains: Critical Size Vias

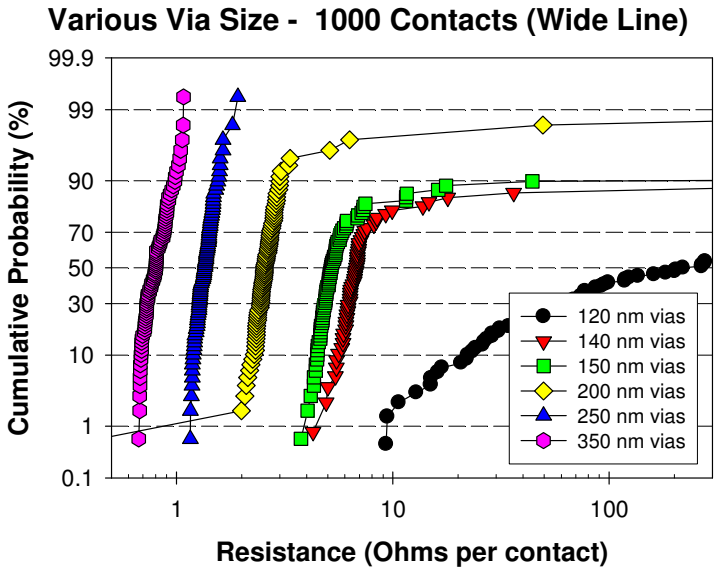
Figure 12.4 (b) and (c) show the cumulative distribution function of the resistance of the 1000-contact via chains of various via and line CDs. In both plots, the via resistance decreases as expected when the via CD increases. This is because smaller cross sectional area leads to higher resistance. Data for the chains of 350 nm vias show excellent yield and data distribution in both via chains with wide and narrow lines. However, for vias smaller than 350 nm in Figure 12.4 (a) and for vias smaller than 250 nm in Figure 12.4 (b), some data clearly deviate to high resistance. In addition, the smaller vias show higher probability of having high resistance data. This indicates loss of yield for these via chains. When the vias of the same size were considered, the loss of yield was found more pronounced for chains with narrow lines than for chains with wide lines.

For via chains with wide lines, the smallest via showing a significant yield is 140 nm, whereas, for via chains with narrow lines, the smallest via CD with significant yield 150 nm. For the 120 nm vias, the data show very high resistance and a poor distribution in the chains with wide lines. The resistance for chains of 120 nm vias on narrow lines is very high and the data are outside the plotting range.

The via size dependence of the chain yield is shown in Figure 12.5. This plot shows a very steep drop in chain yield below a 150 nm via size. The size dependent yield can be explained by the etch bias of the pattern transfer process. This is demonstrated by the following experiment.



(a)



(b)

Figure 12.4: Resistance distribution of via chains: (a) 1000 contacts via chains with narrower lines – line CD 400 nm wider than via CD and (b) 1000 contacts via chains with wider lines – line CD 1.4 µm wider than via CD. Via sizes specified are nominal via sizes on the template. The data for 120 nm vias in (a) are outside the plotting range.

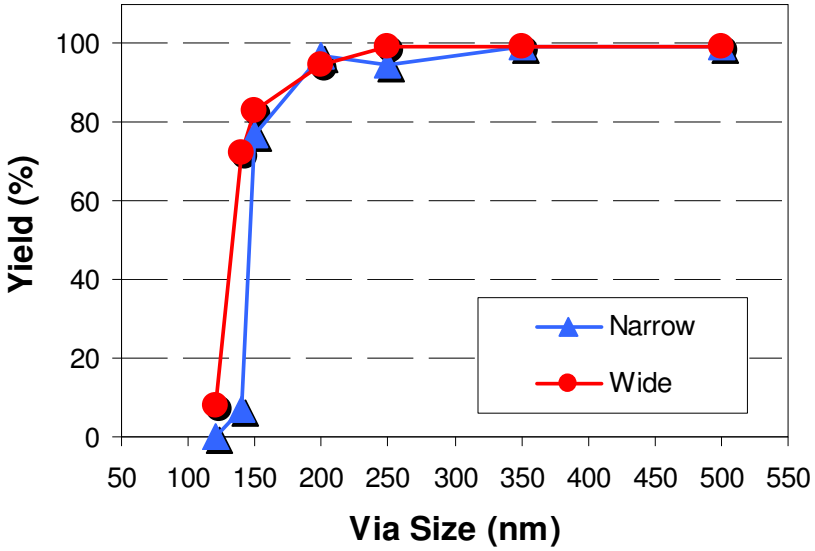


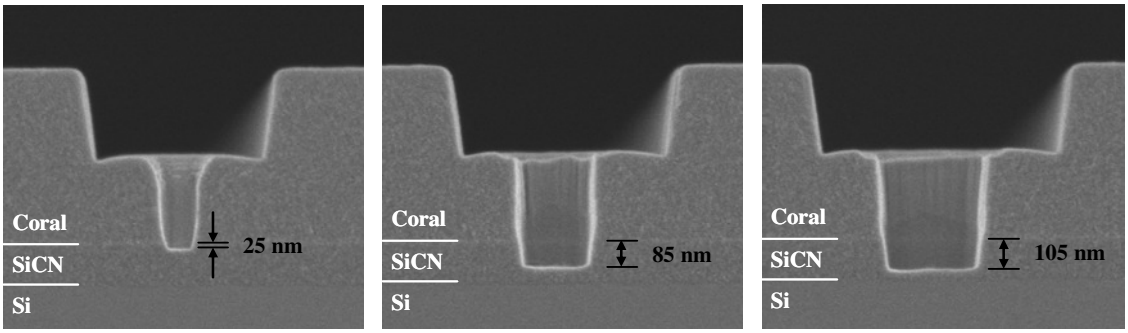
Figure 12.5: Via size and yield of 1000-contact chains

Etch bias experiment

An etch experiment was conducted using the optimum etch recipe on a test wafer with 500 nm low-k ILD and 250 nm SiCN. On the electrically tested wafers, the SiCN cap layer was 12.5 nm thick. The thicker SiCN layer on the etch test wafer in this experiment was intended to investigate whether sufficient over-etch was given to the SiCN cap layer to ensure the clearance of the via contact. Because SiCN is an insulating layer, it must be completely broken through during the etch process in order for the subsequent metallization process to make low resistance contact.

Figure 12.6 shows the result of an etch transfer experiment performed on a test wafer with a thick (~ 125 nm) underlying SiCN cap layer. The SiCN cap layer was only about 12.5 nm thick on the wafers used for electrical testing. Clearly the via etch depths into the SiCN cap layer increase with the via size. For the 350 nm and 250 nm vias, the etch depths into SiCN were 105 nm and 85 nm respectively. The etch depth into SiCN

layer was only 25 nm for the 120 nm vias. There is a correlation between the via CD and etch depth in this etch process. The SiCN etch depth shown on the test wafer is indeed higher than the SiCN layer thickness on the electrical test wafer. In fact, this can be confirmed by the conduction of the Kelvin vias shown in Figure 12.3. However, it is not sufficient to yield the 1000 contact chain. This is because the chain fails when any via in the series fails to make contact with the M1 Cu line. Section 12.3.1.5 describes our efforts to improve the yield of the 120 nm via chains without compromising the feature profile.



(a) (b) (c)

Figure 12.6: Etch bias. Vias are etched to different depths into the SiCN layer due to various via sizes. (a) 120 nm via, (b) 250 nm via, and (3) 350 nm via – SEM courtesy of SVTC, Inc.

Figure 12.7 shows how the average via resistance and yield vary with the number of vias connected in the chain. The Kelvin via structure has the lowest resistance for the following reasons. First, Kelvin vias are single via structures and do not contain the line structures that connect the vias. The data for the via chains were obtained by dividing the total resistance of the via chain by the number of the vias connected. Therefore, the data for the via chains include both the resistance from the vias and the lines, whereas the

data for the Kelvin vias include only the via resistance. Second, the resistance reported for the via chains is by nature the average resistance for these vias whereas the data for the Kelvin vias are reported in a via-by-via fashion. Therefore it is expected that the minimum via resistance data for the via chain will almost always be higher than the minimum resistance for Kelvin vias.

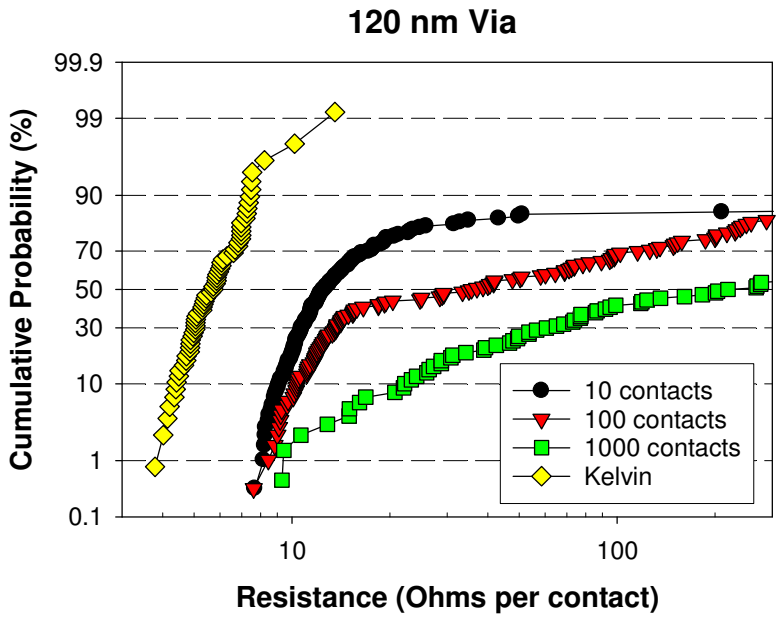


Figure 12.7: Via resistance for Kelvin vias and via chain with 10, 100, and 1000 contacts. Via chains contain line structures that connect the vias and they are 1.52 μm in width. Kelvin vias contain only vias and no lines.

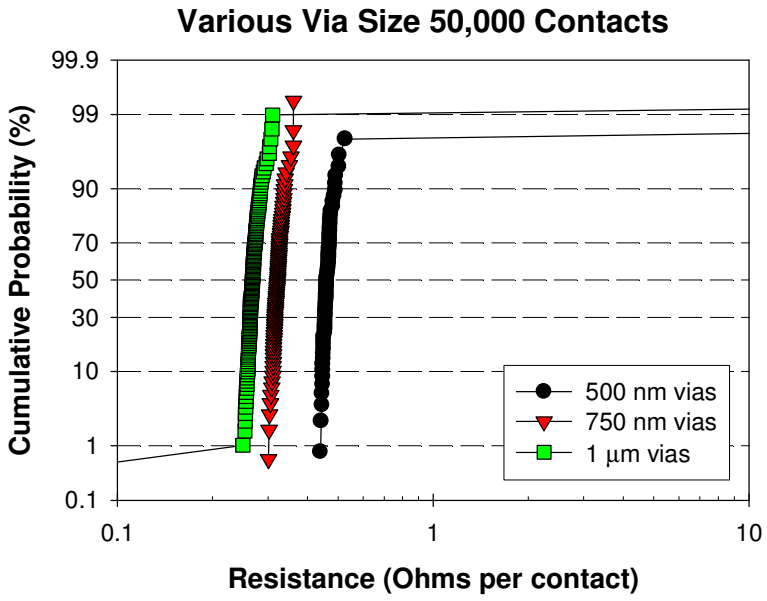
12.3.1.4 Via Chains: Long Chains

In addition to the 10, 100, and 1000 contacts chains, the test vehicle also include chains that are significantly longer, up to 150,000 contacts. As reported in Table 8.2, these long chains contain only large vias, 500 nm to 2 μm. These long chains are also

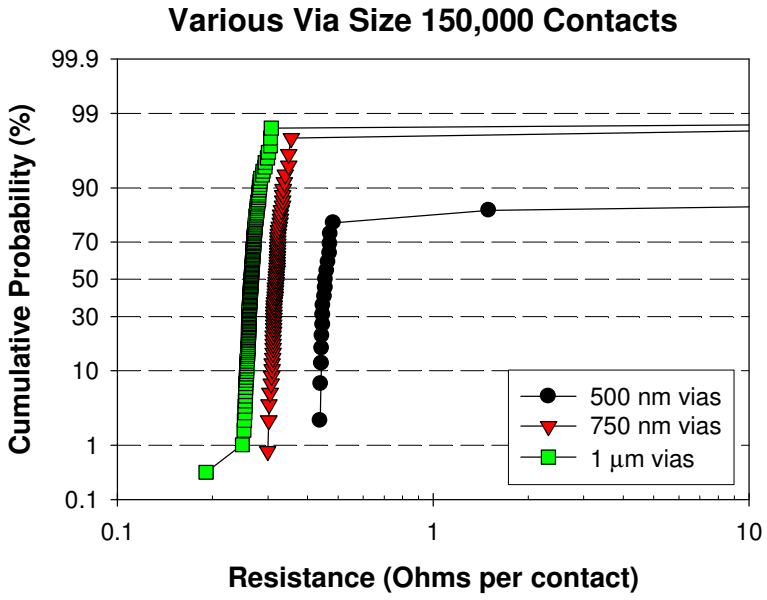
tapped at multiple chain lengths so that shorter chains can also be tested without using additional floor plan.

Figure 12.8 (a) shows resistance of 500 nm, 750 nm, and 1 μm vias in 50,000 contact chains. The via sizes are above the yield drop regime shown in Figure 12.5. The result show excellent yield and data distribution for all three sizes of the vias. Figure 12.8 (b) shows the test result for 150,000 contacts chains. Due to the longer length of the chain, the yield of the 500 nm via chains is reduced to approximately 79%. However, the yield for the 750 nm and 1 μm via chains are still very high. It is interesting to note that there are low resistance tails appearing on the 1 μm via chain data in both Figure 12.8 (a) and Figure 12.8 (b). This is due to incomplete fill of liquid during the imprint process and will be discussed in Section 12.4 along with the results of other experiments.

Figure 12.9 shows the via resistance for long chains with 1,000, 50,000, and 150,000 500 nm vias. The data for 50,000 and 150,000 contact chains are highly consistent with each other except for the expected drop in yield percentage as the respective chain lengths increases. The data for 1,000 contact chains are approximately 20% higher. This is consistent in all experiments conducted on this feature. We could not find plausible explanation for this variance except feature size variation on the template.



(a)



(b)

Figure 12.8: Via resistance for long chains with via sizes 500 nm, 750 nm, and 1 µm, (a) 50,000 contacts, and (b) 150,000 contacts.

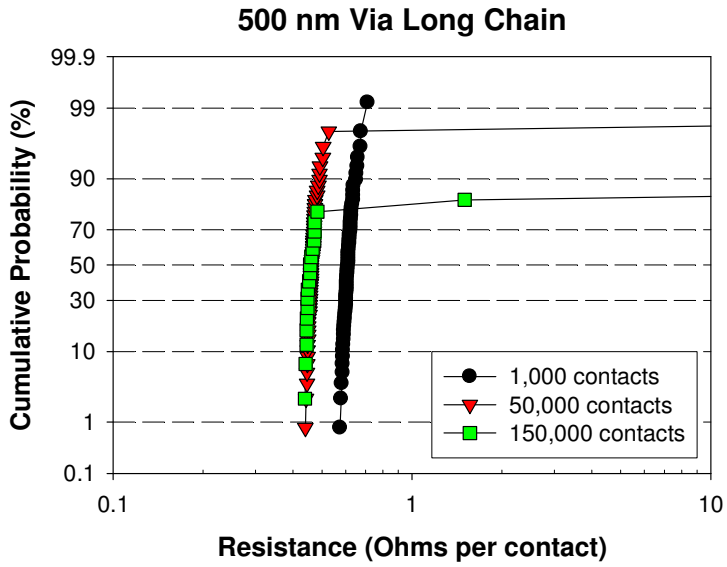


Figure 12.9: Via resistance for long chains with 500 nm vias

12.3.1.5 Discussion

As indicated in Figure 12.5, there was a substantial yield loss below 150 nm vias. This loss results from a via size dependent etch rate, a phenomenon that has been reported many times before [12.2]. Advanced metallization technology is required to improve the yield of the sub 150 nm structures. Many metallization techniques have been reported that drastically reduce via resistance and consequently enhance the yield, such as the barrier-first process [12.3] and the via-punch-through process [12.4]. The barrier first process is a metallization approach in which a layer of Ta(N) is deposited first to protect the via sidewall from resputtering and the substrate RF bias is carefully controlled to render net etch only in the via bottom during barrier deposition [12.3]. The Via-punch-through process is a similar approach, which incorporates an *in-situ* Dep-Etch-Flash (thin Ta) sequence to enhance the protection of the corner at the via entrance from facet formation and ensure the Metal 1 Cu in the via bottom is sufficiently exposed

through extended over-etch for improved electrical contact [12.4]. Both processes are conducted after the completion of dual damascene patterning and before or simultaneously with the barrier deposition.

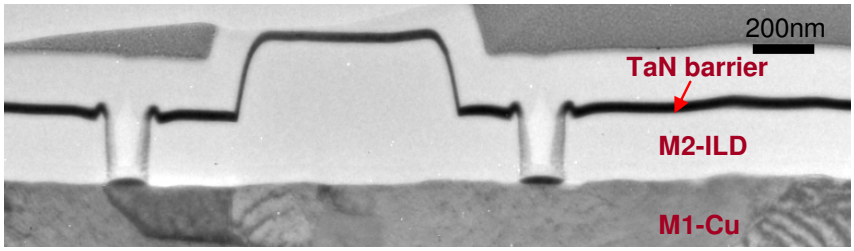
These processing techniques provide very promising routes to solving the yield loss issue of vias smaller than 150 nm in this study. Advanced metallization of this kind requires precise control of substrate bias in the barrier/seed PVD (physical vapor deposition) process because additional ionic bombardment is needed at the wafer surface. Unfortunately, the 200 mm PVD system in SVTC does not have wafer bias capability. Therefore, an experiment was conducted to carry out the via punch through step in an *ex situ* manner in the plasma etcher (Tokyo Electron Unity II E).

Figure 12.10 shows the Transmission Electron Microscopy (TEM) images of the 110 nm dual damascene structures that were produced with SVTC's dual damascene process using photolithography. Although the dual damascene feature in this experiment was made by photolithography, the result of the *ex-situ* via punch through process can be applied to the metallization step of the multi-level S-FIL dual damascene process. This wafer was subjected to the following two processing steps.

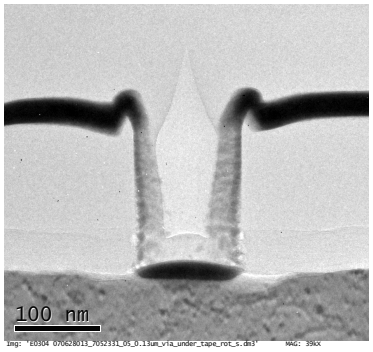
(1)	Barrier deposition	PVD system	30 nm TaN deposition
(2)	Ar resputter	Plasma etcher	20 mT/1500W/100% Ar

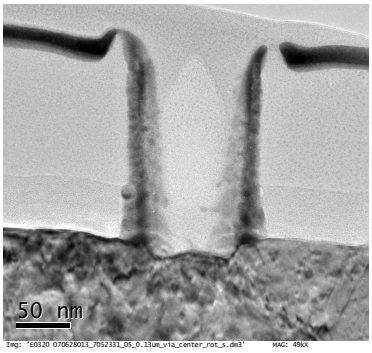
Figure 12.10 (a) shows the image of the dual damascene feature after the TaN barrier deposition, that is, step (1). Figure 12.10 (b) shows only the via area of Figure 12.10 (a). In this particular via, the TaN barrier at the via bottom appears to be in direct contact with Metal 1 Cu. However, dielectric residues can be present at the contact between the barrier and Metal 1 Cu due to etch residues or uncleared cap layer. Such

residues can increase the via contact resistance and therefore suppress the via chain yield. Since fluorocarbon based etch chemistry produces fluorocarbon polymer deposition, a physical etch process that can etch into Metal 1 Cu is likely to provide an effective solution to the contact cleaning process. Figure 12.10 (c) shows the TEM image of the via after the Ar only physical etch, that is, step (2). The TaN barrier at the via bottom was clearly removed and the Ar process etched approximately 10 nm into the M1-Cu. The via contact is expected to be completely cleared of the etch residues since the Ar punch through step is a physical sputtering process. This experiment showed that the via contact can be etched into the underlying Metal 1 Cu to improve electrical contact without compromising the profile of the dual damascene feature.



(a)





(b) (c)

Figure 12.10: *Ex-situ* via punch through experiment: (a) and (b) before via punch through, and (c) after via punch through – TEM courtesy of SVTC, Inc.

Figure 12.11 describes how this is achieved by the concurrent sputter and redeposition of the barrier material during the *ex-situ* via punch through process. Inside the high aspect ratio vias, the ionic bombardment can reach the via the bottom because it is a line of sight process. The resputtered barrier material however will predominantly land on the via sidewall. This is shown in Figure 12.11 (a). Outside the high aspect ratio vias, the etch rate is lower than the via bottom because there is concurrent sputter etch and redeposition on the horizontal surfaces. The overall etch and deposition effects are shown in Figure 12.11 (b). The via bottom is subject to etch only because the shadowing effect significantly suppresses the redeposition. The result is a higher etching rate at the via bottom compared to other surfaces. The dual damascene profile is therefore conserved during the via punch through process.

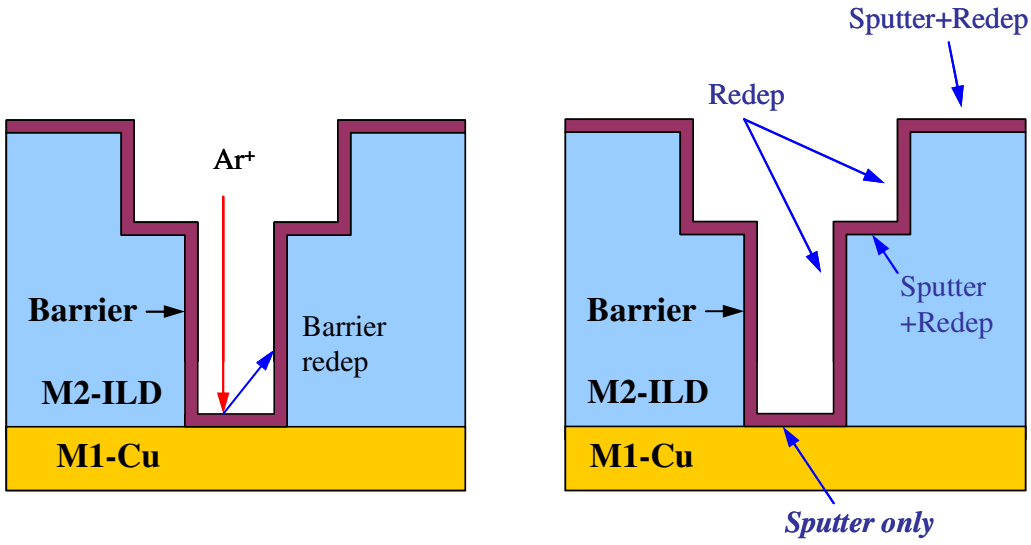


Figure 12.11: Concurrent sputter and redeposition of barrier material during *ex-situ* via punch through process. (a) Effect at via bottom and (b) overall effects on all surfaces.

The result shown in Figure 12.10 clearly indicates that the via contact can be cleared by the *ex-situ* via punch through process. The contact resistance is expected to be low since the physical etch process does not induce any polymer deposition. In addition, the dual damascene feature shape can be protected and faithfully preserved. However, we could not pursue yield enhancement by this technique because it requires an etch chamber dedicated to such a process that can handle 8 inch wafers and this was not available in SVTC. Therefore, we could only pursue yield optimization through other routes. These are discussed in next section.

12.3.2 Process Version II: Optimal Via Yield

12.3.2.1 Feature Profile

An alternative to optimize the via yield is to intentionally increase the via facet and reduce the via height, thereby exposing the bottom of the via to more effective "cleaning". This process utilized a line etch chemistry that has lower C_4F_8 proportion in the etch chemistry, which caused tapering of the via sidewall. This recipe is reported in Table 12.1. The recipes for the other etch steps were identical to the recipes reported in Table 10.2.

Table 12.1: Recipe for line etch step in the process that intentionally tapered via for yield improvement

Etch Step	Pressure (mT)	Power (W)	Etch Gases (% total flow rate)		
Line Etch	75	400	2% C_4F_8	50% CF_4	48% N_2

This was the only approach we could explore within the framework of the equipment setup available for 8 inch wafer processing in SVTC. With the new process, the smallest resulting via structure, generated from 120 nm feature on template, has an 83 nm final CD in the via bottom and is 140 nm in height, as shown in Figure 12.12.

12.3.2.2 Via Chains: Critical Size

The via chain resistance of the tapered via process is shown in Figure 12.13. The yield of the via chains of intermediate and small CD have greatly improved from that shown in Figure 12.4. For the 1000 contact via chains with the smallest via structure on this template, 120 nm in template CD and 83 nm in the final via bottom CD, 97.6% yield were achieved for chains with 520 nm lines and 94.4% yield for chains with 1.52 μm lines. Before the yield optimization, the yield of these features was negligible, as shown in Figure 12.4 and Figure 12.5. In addition, the resistance has significantly less variation across all via sizes tested.

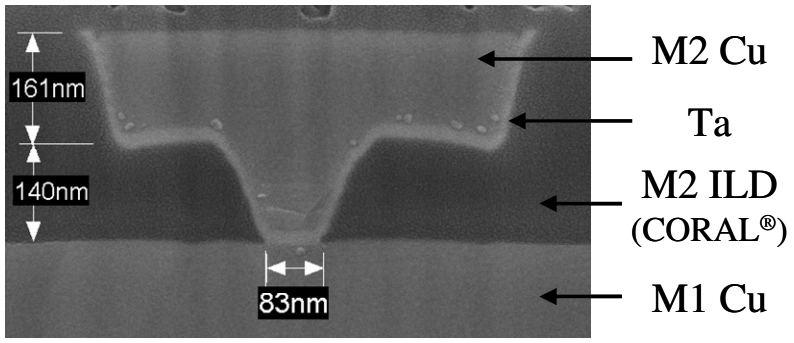
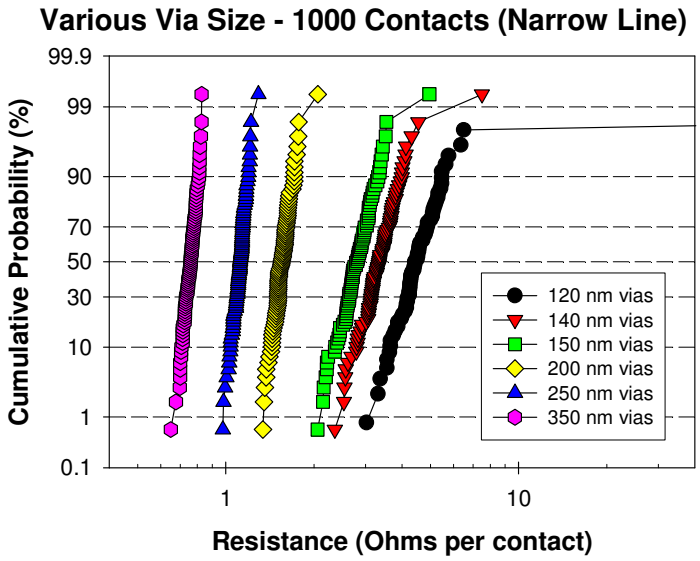
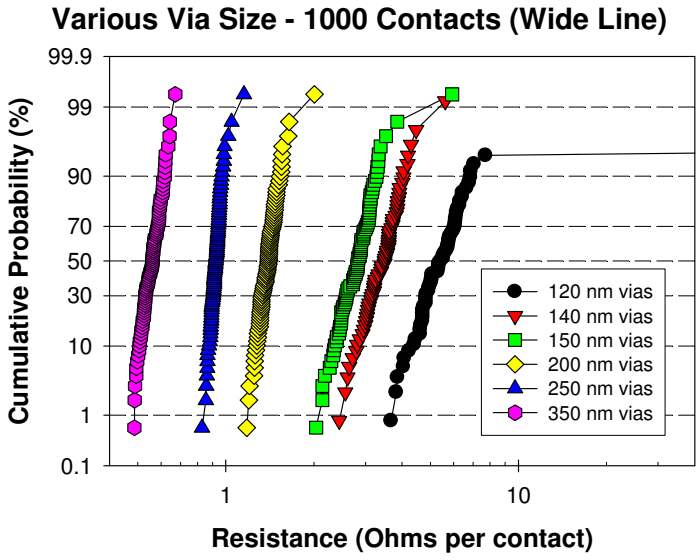


Figure 12.12: Dual damascene feature of nominal 120 nm via. Final via bottom CD = 83 nm, height = 140 nm. Purposely tapered via and reduced via height for yield optimization on 8 inch wafer processing tool set – SEM courtesy of SVTC, Inc.



(a)



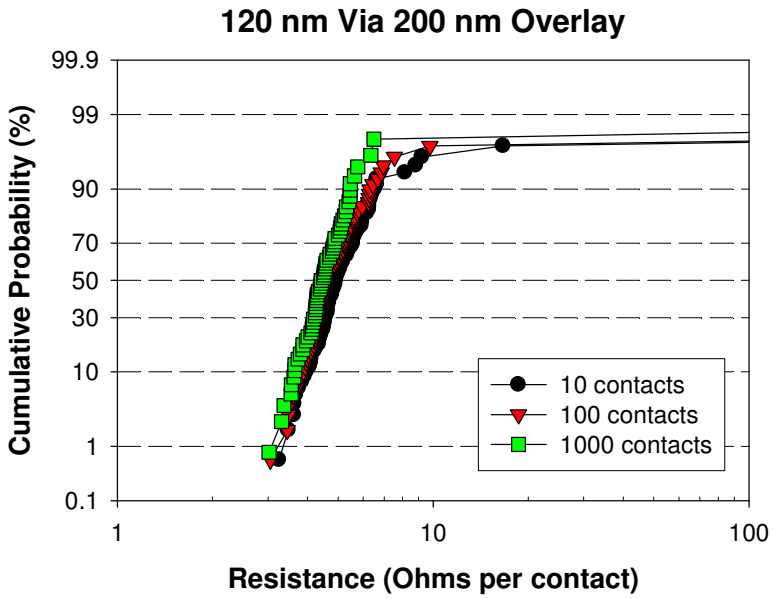
(b)

Figure 12.13: Via resistance of 1000 contact chains of various via CD: (a) via chains with narrower lines – line CD 400 nm wider than via CD and (b) via chains with wider lines – line CD 1.4 µm wider than via CD. All sizes specified are nominal sizes.

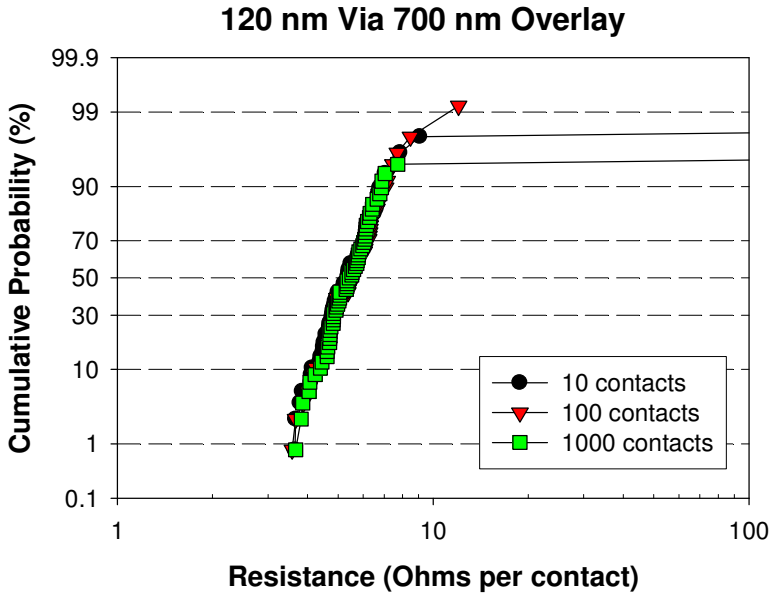
Figure 12.14 shows the via resistance of the 120 nm vias in chains with 10, 100, and 1000 contacts. The results obtained from different chain lengths are very consistent. Figure 12.7 shows the same plot for the chains with wide lines (1.52 μm) before the process improvement. The data for chains with narrow lines were not plotted because the result was nearly complete electrical open for all features tested. It is apparent that values and distribution of resistance data in Figure 12.14 have improved drastically from those in Figure 12.5 as a result of the tapered via process.

12.3.2.3 Via Chains: Long Chains

Figure 12.15 (a) shows resistance of 500 nm, 750 nm, and 1 μm vias in 50,000 contact chains. The yield of these large vias was already very high in the original process, as shown in Figure 12.8 (a). The improved process did not cause any major change in the resistance distribution of these large vias. However, the resistance values are lower due to the shortened via height created in the new process. Figure 12.15 (b) shows the result for the large vias in 150,000 contacts chains. All sizes show good yield with the new process compared to the result with the original process shown in Figure 12.8 (b). In both Figure 12.15 (a) and (b), the low resistance tails for 1 μm via chains appear more pronounced than they appear in Figure 12.8 (a) and (b). The root cause for the low resistance tail is the imprint process and not the integration. This will be discussed in Section 12.4.

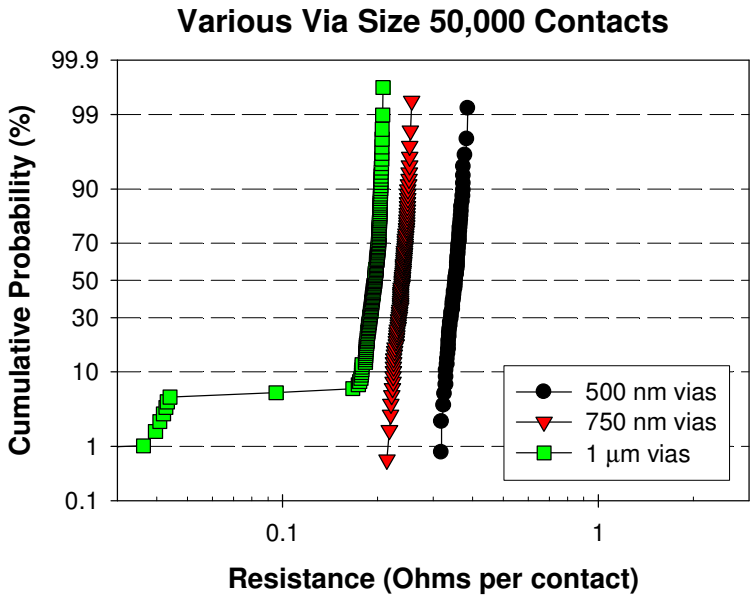


(a)

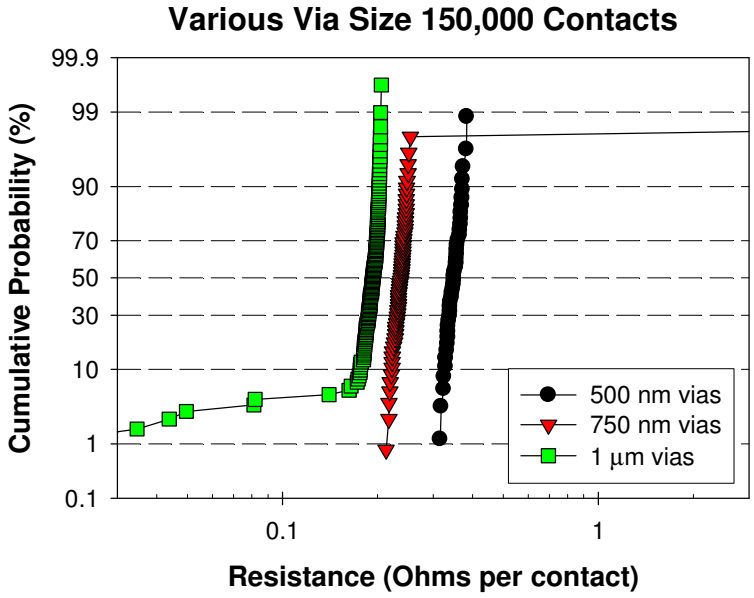


(b)

Figure 12.14: Via resistance of 120 nm via chains with 10, 100, and 1000 contacts on (a) narrow lines and (b) wide lines.



(a)



(b)

Figure 12.15: Via resistance for long chains with via sizes 500 nm, 750 nm, and 1 µm. (a) 50,000 contacts, and (b) 150,000 contacts.

Figure 12.16 shows the via resistance for long chains with 1,000, 50,000, and 150,000 500 nm vias. The data not only show excellent yield but also a very tight distribution. All data falls inside the main distribution without any deviation indicating that the yield of these features far exceeds the statistics shown in the test. Compared to the corresponding plot for the original process in Figure 12.8, the optimized process shows improved results in yield, data distribution, and resistance. Similar to the original process, it is also observed here that the via resistance of 50,000 contact chains and 150,000 contact chains are nearly identical, while the resistance of 1,000 contact chains is approximately 25% higher. As discussed in previous section, there is no plausible explanation except feature size variation on the template.

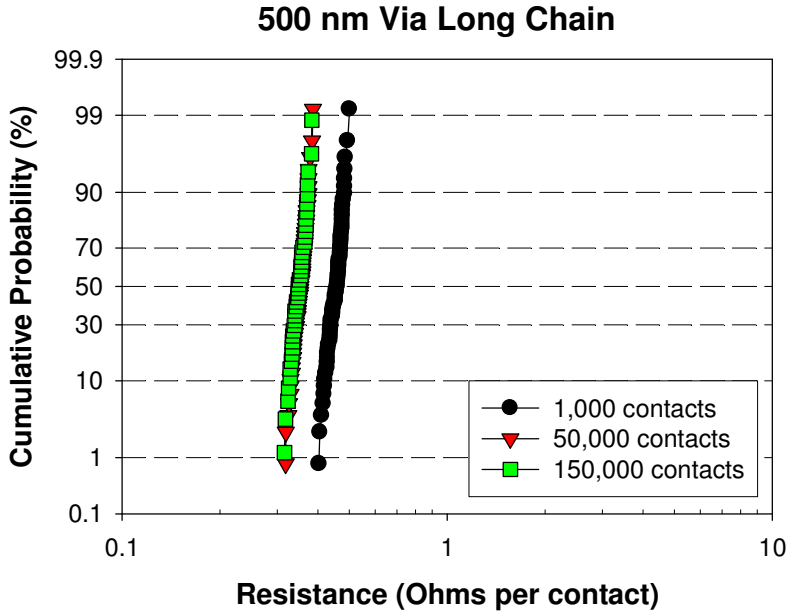
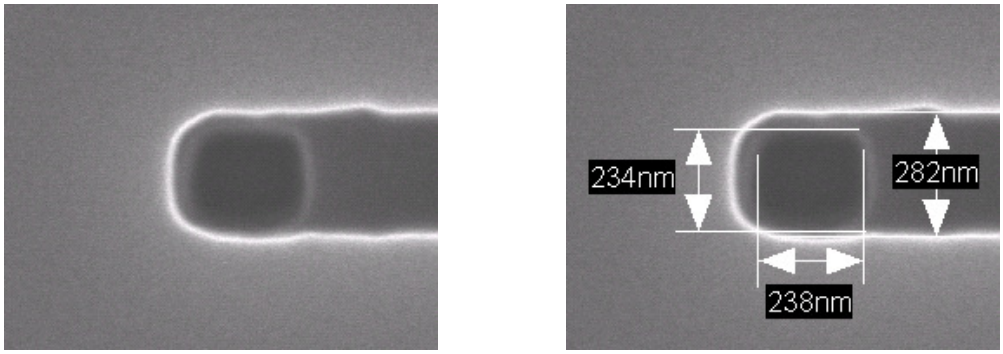


Figure 12.16: Via resistance for long chains with 500 nm vias

12.3.2.4 Discussion

This process provides excellent yield across all sizes on the template. There are, as described earlier, more attractive ways to improve the yield without compromising the feature profile, but these processes require tools that were not available for 8 inch wafer processing in SVTC, Austin TX. Although significant improvement in yield was achieved, the intentionally tapered dual damascene feature profile (Figure 12.12) raises some concern over the critical dimension change. This can be studied using the dual damascene features with the vias and the lines of the same size. Structures like this represent the arrangement of highest feature density of a given via size. Feature density will be compromised if the critical dimension increases due to the via taper.

Figure 12.17 shows a top-down SEM image of the imprinted dual damascene feature designed to have the same size for the vias and the lines. By design, this is a feature with 250 nm vias and 250 nm lines. As shown in Figure 12.17 (b), the imprint pattern is 282 nm in line width. The via is approximately rectangular, 238 nm in the direction parallel to the line and 234 nm perpendicular to the line.



(a) (b)

Figure 12.17: Top down image of imprint pattern of nominal 250 nm via / 250 nm line dual damascene structure: (a) SEM image, and (b) SEM image with metrology – SEM courtesy of SVTC, Inc.

Figure 12.18 shows the same dual damascene feature, with nominal 250 nm via 250 nm line after the pattern transfer and metallization processes. The cross section was conducted in two directions, perpendicular and parallel to the line, in order to investigate the critical dimension change in these two directions. Figure 12.18 (a) and (b) show the diagram depicting perpendicular and parallel cross section. The directions of observation with SEM are shown in both figures as broad purple arrows.

The feature width perpendicular to the line direction is the most critical dimension. A lateral CD increase can cause a significant increase in line to line capacitance because the capacitance is approximately inversely proportional to the dielectric thickness between two adjacent conductors. Shorting between neighboring lines is also possible. Therefore, the lateral CD increase limits the feature density when the lines are aligned in dense arrays. Figure 12.18 (c) and (d) show the SEM images in the perpendicular cross section. While the imprint pattern shows the via lateral width to be 234 nm and line width to be 282 nm, the via and line have the same width of 189 nm in both the via and the line level of the feature after the metallization. This shows that a decrease, rather than an increase, was observed in later CD. This result shows that the taper via process will not affect the array density that is critical to the BEOL technology.

As shown in Figure 12.12, this process causes the via to taper when the line structure is wider than the via. Interestingly, when the line is approximately the same size as the via, the via and line sidewalls remain vertical. The average sidewall angle is over 89° as indicated in Figure 12.18 (d). This observation can be explained as follows and in Figure 12.19.

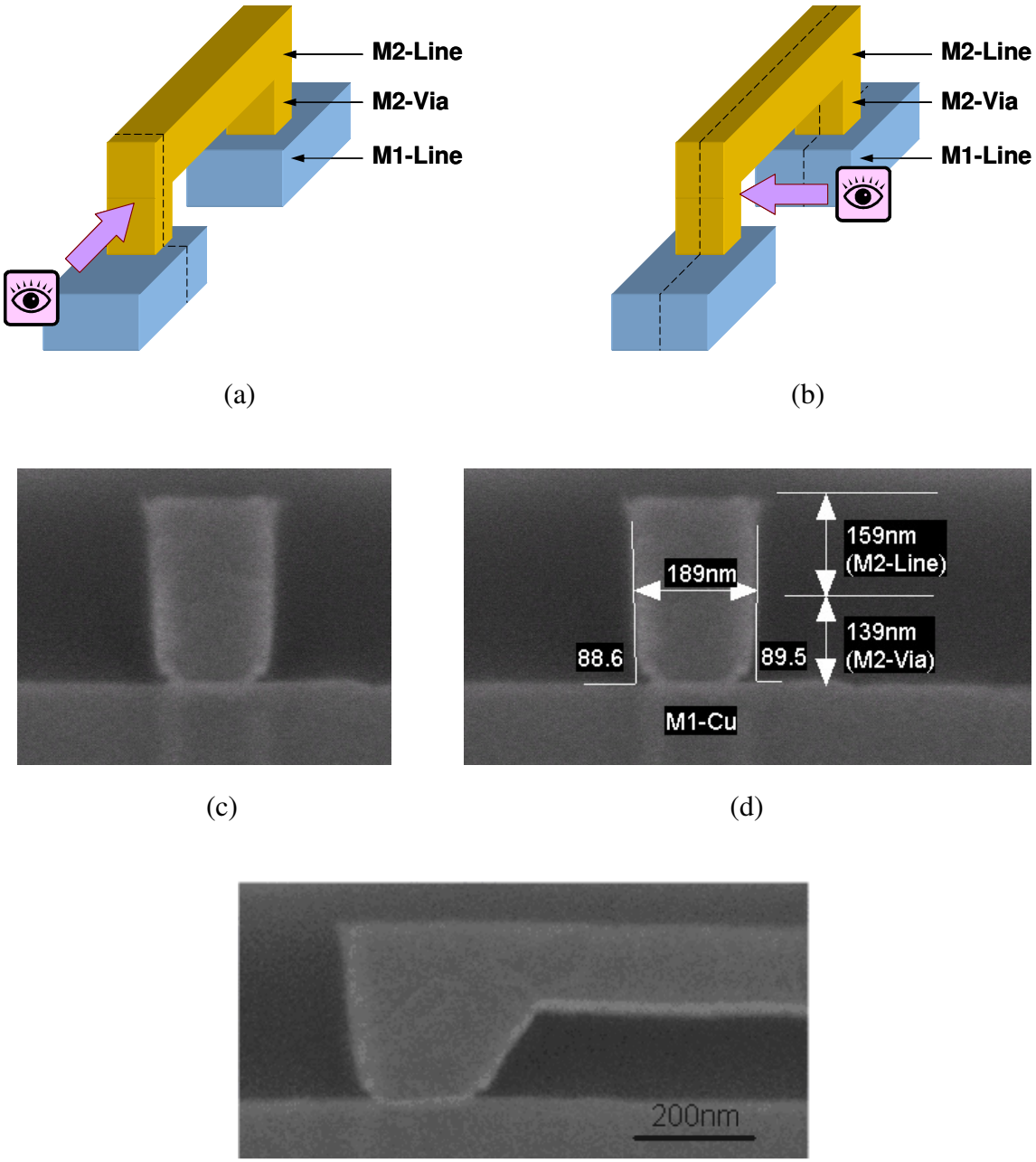


Figure 12.18: Dual damascene feature with 250 nm via and 250 nm line: (a) cross section perpendicular to line, (b) cross section parallel to line, (c) and (d) perpendicular cross section SEM, and (e) parallel cross section SEM. Dotted lines in (a) and (b) indicate cross section direction – SEM courtesy of SVTC, Inc.

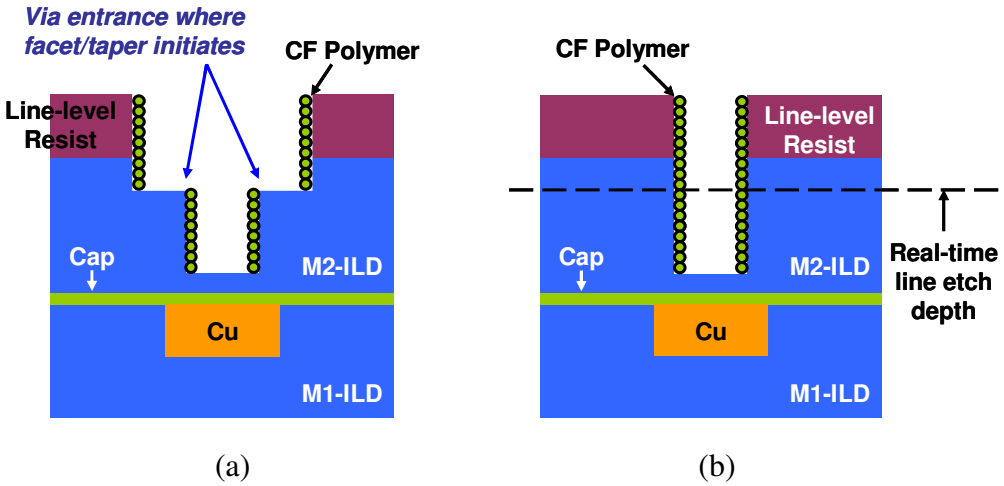


Figure 12.19: Line etch and line-to-via size difference: (a) line width > via size, and (b) line width ≈ via size

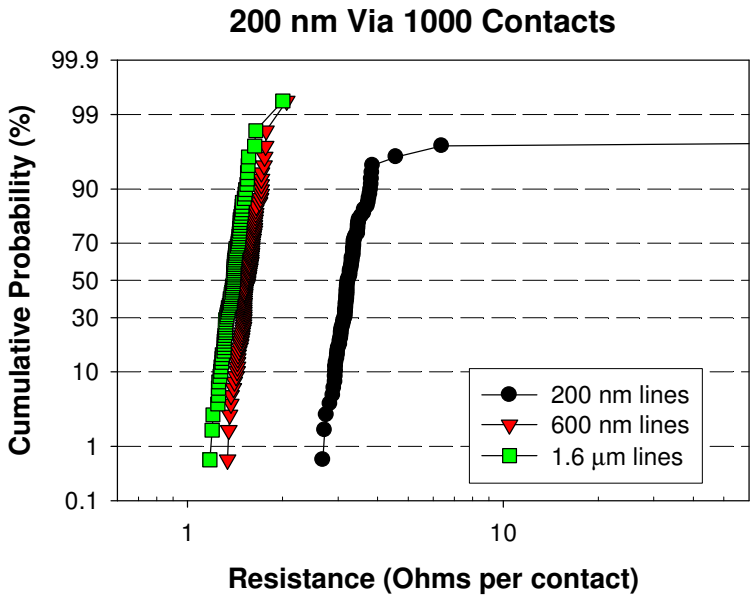
Figure 12.19 shows two dual damascene features at the same stage of the line etch step. The line width is larger than the via size in Figure 12.19 (a), corresponding to the SEM image in Figure 12.12, whereas the line width and the via size are approximately the same in Figure 12.19 (b), corresponding to the SEM image in Figure 12.18 (c). The top surface of the via entrance lacks the protection of the sidewalls and the facet or taper can initiate at the corners as shown in Figure 12.19. Therefore, maintaining vertical sidewalls requires precise control of the etch chemistry. However, when the line width is equal to the via size, there are no vulnerable corners exposed and all sidewalls are protected by the fluorocarbon polymer deposition. Under this condition, controlling the sidewall taper becomes less difficult and the etch process window for vertical sidewalls is significantly wider.

Figure 12.18 (e) shows the parallel cross section SEM image of the dual damascene feature. The sidewall is again tapered with the tapered via process. This is

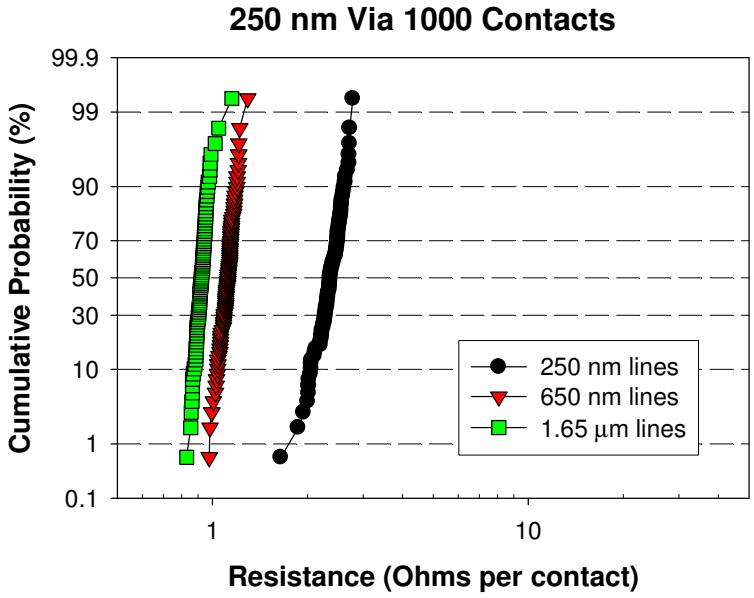
because of the exposed corner as in Figure 12.19 (a). Fortunately this taper occurs parallel to the line and therefore does not affect the feature density.

Figure 12.20 shows the via chain resistance of the 200 nm and 250 nm dual damascene structures. Both plots contain a set of data obtained from the structure with equal line width and via size. The final CDs for the structures with equivalent line and via sizes are 155 nm and 183 nm respectively. Apparently resistance is higher for these structures due to the CD decrease and lack of lateral via taper. The yield is good and there is good data distribution. However, the yield tops off at 97% for nominal 200 nm structure with equivalent line and via sizes. This raises one interesting question. The tapered via process was adopted to improve the via chain yield based on the 200 mm wafer processing tool set that was available for this study. It is pleasing to find that the via taper process can create vertical sidewalls as long as the line and the via widths are equivalent. However, if the yield is suppressed under this condition, the advantage of equivalent line and via CD is cancelled. Unfortunately, this question remains unanswered in this study. The smallest via chain structure with equivalent line and via CDs on this template is 200 nm by design. Incidentally this is the size just above the yield loss regime in the original, non-tapered process. Therefore the yield of structures with equivalent line and via CDs can not be verified for the most critical sizes, which are below 150 nm.

Overall, the via taper process significantly improves the yield, resistance, and data distribution across all sizes of the via chains tested. Although the via is tapered in some dual damascene structures, it was observed that the via sidewalls remain vertical as long as the line and the via CDs are equivalent.



(a)



(b)

Figure 12.20: Via resistance for 200 nm and 250 nm via chains with various line width: (a) 200 nm via chains, and (b) 250 nm via chains

12.4 FAILURE ANALYSIS

In addition to the study of the yield of the via chains, it is also important to investigate how the features that have low yield correlate with specific failure modes. This section describes the correlation we have observed in this study.

12.4.1 Electrical Open-Circuit Failure

Electrical open is the failure mode the via chains are designed to capture. The electrical test measures the chain resistance, an unreasonably high resistance value occurs if any one or more vias fail to make contact with the M1 Cu lines. However, it was observed that a few via chains invariably showed 100% electrical open no matter what kind of process the wafer received. SEM analysis revealed that in this case at least one via is missing from the chain. This is shown in Figure 12.21. In this study, there was not enough evidence to identify the root cause of these missing vias. However, due to the repeatability of these failures, it was concluded that they resulted from the template, rather than the imprinting or subsequent processing steps. Therefore, the data obtained from these identified defective chains were not included in the analysis presented in above sections. This is because the objective of this study focuses on demonstrating the integration of multi-level S-FIL with standard BEOL processing, not the production of a perfect template.

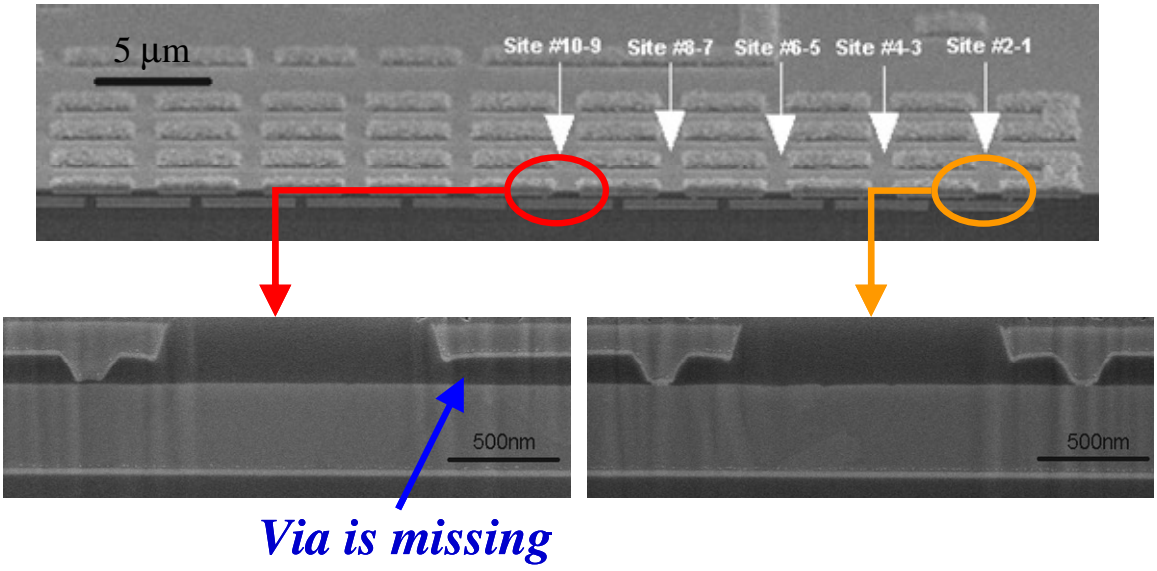


Figure 12.21: Nominal 120 nm via chain with at least one missing via – SEM courtesy of SVTC, Inc.

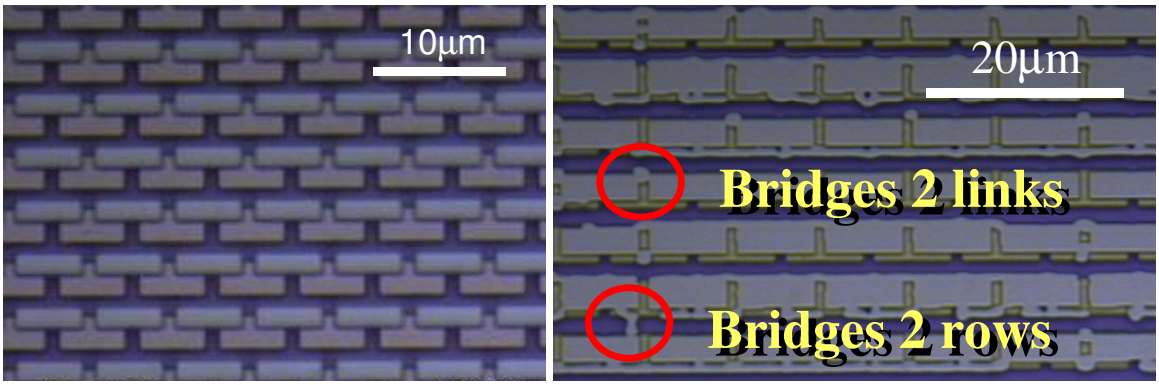
12.4.2 Electrical Short-Circuit Failure

12.4.2.1 Description

Short-circuit failure is the failure mode unique to imprint lithography. Unfortunately, detection of this kind of failure is challenging with the standard via chain test structures. In photolithography, patterns are generated by first exposing the photoresist to a pattern of light and subsequently dissolving the exposed region in a developer. Therefore, if the image fails to resolve, the pattern area will not dissolve and the photoresist will remain on the wafer. After the pattern-transfer etching process, the intended features at the unexposed area will be missing and produce an open in electrical testing. However, for imprint lithography, patterns are generated by the liquid monomers filling the pattern cavity under the template. When an image fails to resolve, the failing areas are devoid of resist material. Therefore, after the pattern transfer

etching process, additional and unintended Cu features will be created and produce a short in electrical testing.

Figure 12.22 (a) shows the top-down image of a normal via chain using an optical microscope. This wafer had completed the M1 and M2 processing flow. The M1 Cu lines are shown in the bottom layer and the M2 Cu lines are shown in the top layer. The imprint process was successful. Figure 12.22 (b) shows an abnormal via chain due to an unsuccessful imprint process that had incomplete filling issues. After the metallization processes, additional and unintended features were produced. These features are consistent with those observed in Figure 9.2.



(a) (b)

Figure 12.22: Via chains after complete M2 metallization: (a) the imprint process was normal and all features were resolved, and (b) the imprint process was abnormal and additional features were created between intended features

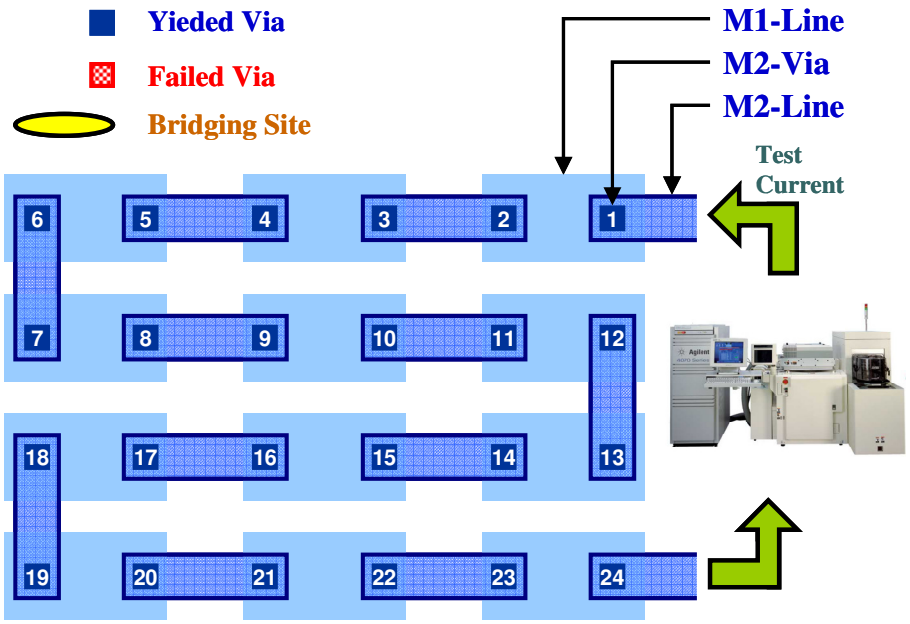
For the via chains patterned with photolithography, a bad process leads to missing vias or lines and will cause electrical-open circuit failure detectable by the standard resistance measurement. For the via chains patterned with imprint lithography, a bad process creates additional features which provide additional paths for the test current and

therefore decreases the overall resistance of the chain. When the creation of additional features is pervasive, the resistance decrease will be pronounced, as indicated by the low resistance tail in Figure 12.8 and Figure 12.15. However, when only few additional features are created in a relatively long chain, the resistance decrease is minimal and will be difficult to identify given the resistance variation due to other effects.

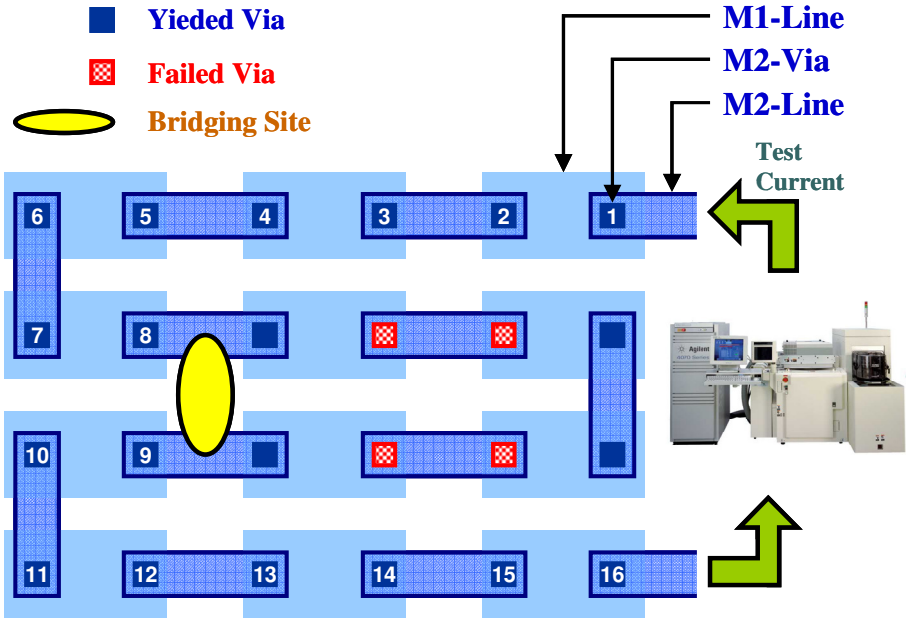
Most important of all, significant uncertainty arises in the verification of the via yield with via chain testing. Figure 12.23 (a) shows the conduction in a chain resistance test of a normal chain. The test current flows through via #1 through #24 and the chain resistance will be the sum of the 24 tested vias. Conduction of the chain indicates yield of all 24 vias in the chain. Figure 12.23 (b) shows the conduction of an abnormal chain with a bridging site similar to the experimental observation shown in Figure 12.22 (b). Two misinterpretations of the test data could be obtained.

Scenario 1

Four of the vias contained in this chain are defective and no electrical contact was made through them. However, the test current was bridged through the additional feature and skipped the defective via. The electrical test result indicates conduction despite the four electrical open vias. Therefore, the yield of the via chain is overestimated.



(a)



(b)

Figure 12.23: Via chain resistance test: (a) a normal chain, and (b) a chain with a bridging site due to defective imprint process

Scenario 2

Even if all vias in the chain have good electrical contact, the majority of the test current can still flow through the bridging site and skip a number of vias. Instead of measuring the resistance of 24 vias, the electrical test in fact detects the 16 vias on the lowest resistance route. Therefore, the via chain resistance is underestimated.

A microscopic canvass of the die could detect these short-circuit defects. However, such practice is impractical and contradicts the purpose of yield determination using electrical testing. In order to capture the imprint specific defect, it is essential to redesign the test structure. Two new test structures are proposed in next section for this purpose.

Finally, it is also interesting to point out that, if bubble formation can be correlated with the low resistance tail in Figure 12.8 and Figure 12.15, one can easily observe that such defects are mainly observed at the via chains with large via sizes. Research showed that bubble formation mainly occurs by two mechanisms; feature pinning and drop encircling [12.5]. In this study, the occurrence of the low resistance tail is feature specific. We processed 8 E-test wafers using slightly different etch processes. Data from two of them were presented in this chapter. However, in all 8 E-test wafers, the low resistance tails predominantly occurred in the via chains of the size 750 nm or above. It very rarely occurred in the via chains below 500 nm. The feature specific characteristic of the low resistance tail seems to indicate the possibility of a feature pinning effect. Liang *et al.* [12.5] also showed that large bubbles can take very long time to dissolve. This appears to correspond with the finding in this dissertation, provided some correlation exists between the size of the bubble pinning feature and the size of the bubble.

12.4.2.2 Interwoven Via Chains

In order to detect the short circuit bridging between adjacent links, the design strategy is to arrange the chains in an interwoven fashion so that the neighboring links belong to an otherwise insolated chain. Figure 12.24 shows the basic design of the interwoven chains. The test structure contains two independent via chains: chain A (blue) and chain B (green). Each chain has two terminals for testing. Both chains can be tested independently as a standard via chain. A cross chain test, e.g. terminal A1 to terminal B1, detects the bridging feature between adjacent rows. This design is unable to detect bridging in the direction parallel to the lines because the neighboring links in this direction in fact belongs to the same chain. However, this chain design closely resembles the standard via chain. The patterns in the M1 level are identical to the standard design. At the M2 level, only the leftmost and rightmost links are different from the standard design. Therefore, this structure is the easiest to implement.

Figure 12.25 shows the interwoven chains with a comb structure interdigitated between adjacent links in the parallel direction. The two chains and cross row bridging can be tested with the basic interwoven chain. Conduction between one of the chains and the comb structure, e.g. A1 to Comb, detects the bridging between links in the parallel direction.

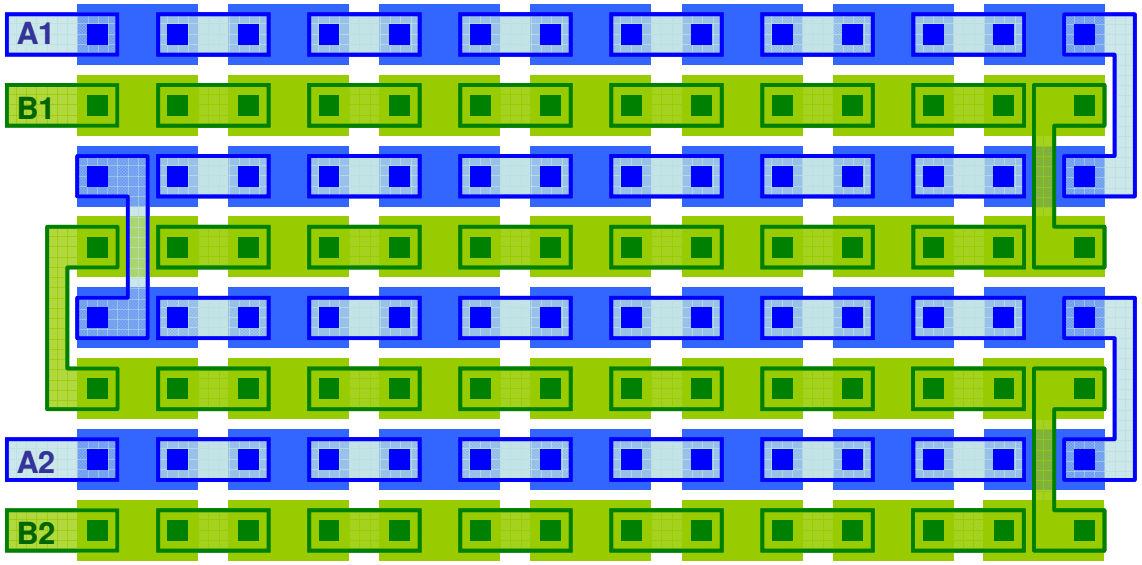


Figure 12.24: Interwoven chains. The solid rectangles are M1 lines, transparent rectangles are M2 lines, and the solid squares are the vias. The comb structure is at the M2 line level.

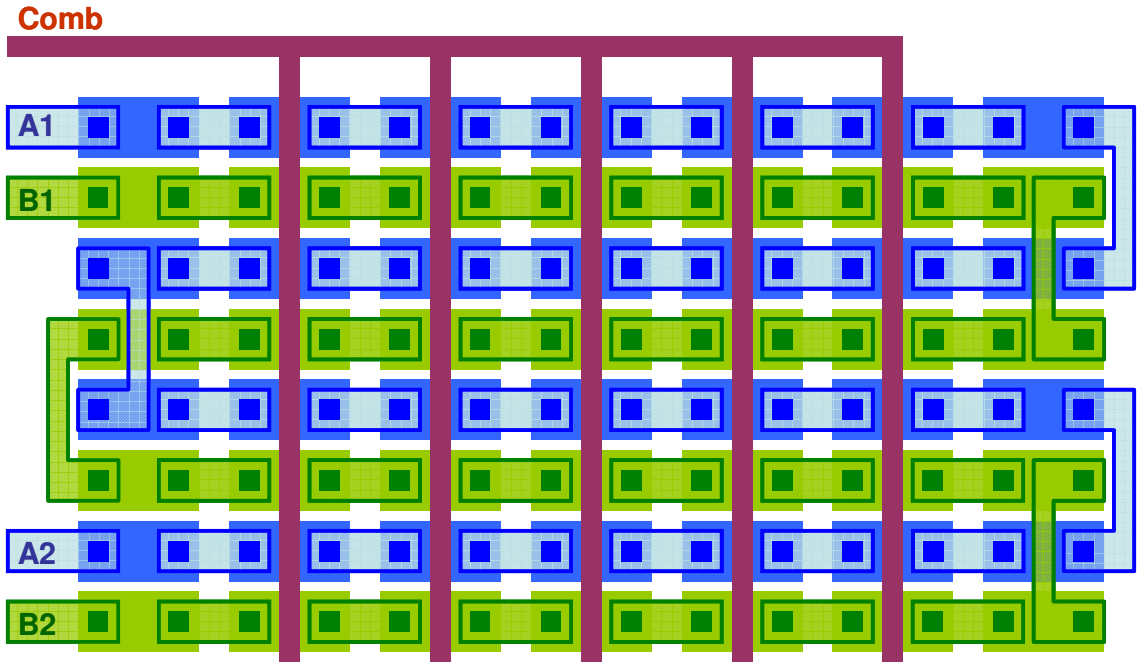


Figure 12.25: Interwoven chains with a comb. The solid rectangles are M1 lines, transparent rectangles are M2 lines, and the solid squares are the vias. The comb structure is at the M2 line level.

12.5 CONCLUSIONS

The yield results substantiate that multilevel S-FIL in conjunction with the *in-situ* multistep etch scheme indeed provides a high-resolution, high-yield, and low-cost patterning process for Cu low-k dual damascene products. It is also fully compatible with a current industry-accepted BEOL process flow and was demonstrated on imprint tools and resist materials that are commercially available. Improvements are available in advanced imprint tools with high resolution inkjet dispense for S-FIL and etch tools that enable the via punch through processes. Therefore, there is the opportunity for significant improvement.

Chapter 13: Conclusions

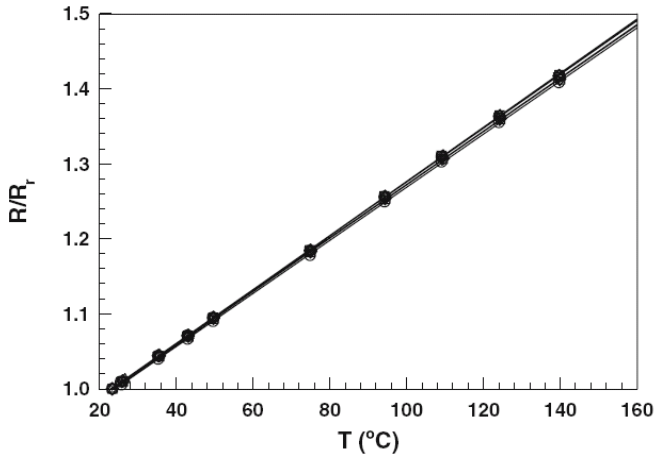
In this study, a Cu/low-k Back End Of the Line (BEOL) dual damascene process was demonstrated using multilevel Step and Flash Imprint Lithography (S-FIL). The Step and Flash Imprint Lithography process provided high resolution and high pattern fidelity, and was adjusted to provide low residual layer thickness and high imprint uniformity. Multilevel Step and Flash Imprint Lithography is capable of patterning the via and the line structures in one single imaging step. This significantly reduces the complexity of the conventional dual damascene processing and provides great cost saving by reducing the number of processing steps. The etch process required to transfer the multilevel patterns into the dielectric material emerged as a technical challenge. An etch scheme was developed to enable the multilevel pattern transfer. This new approach performs the etch in a step-wise, *in-situ* fashion, and provides excellent pattern fidelity, a wide process window and minimal etch artifacts. High electrical test yields were obtained for the via chains made with multilevel S-FIL and multi-step etch scheme. The result demonstrates the viability of Step and Flash Imprint Lithography as a candidate for integration into BEOL dual damascene processing. In addition, imprint-specific issues were identified that are pertinent to the process, test methods, and yield. New test structures were proposed to address these issues.

Appendix A: Joule Heating of the Electromigration Experiment

In order to account for the Joule heating that raises the temperature of the solder bump under current stressing, the following tests and modeling were conducted. The experiments were conducted by Seung-Hyun Chae, the simulation was conducted by Xuefeng Zhang, and the results were reported in Ref [2.5].

First, resistance of the test structure was measured at various oven temperatures using minimal current (50mA). It was assumed that the effect of Joule heating was minimal and the solder temperature was equal to the oven temperature when the test was conducted at such low current. The result is shown in Figure A.1. The temperature coefficient of resistance (TCR) and the following relationship were obtained.

$$\frac{\Delta R}{R_r} = 3.6\times10^{-3}\left(T - T_r\right) \tag{A.1}$$



(Source: S. –H. Chae *et al*. in Ref [2.5])[11]

Figure A.1: Plot of R/R_r with temperature (R is the resistance of the test structure measured at a given temperature, and R_r is the resistance measured at room temperature).

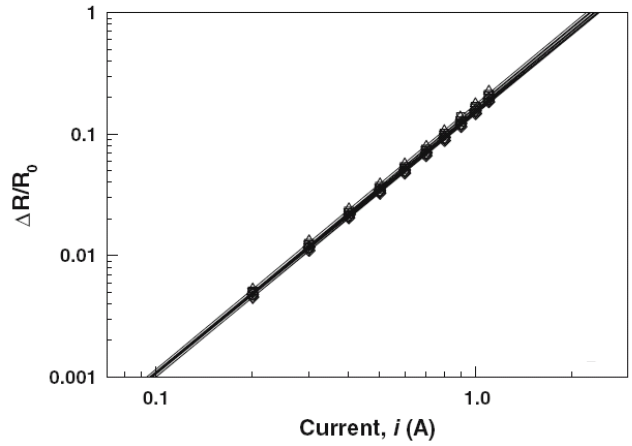
[11] With kind permission from S.-H. Chae, Master Report, the University of Texas at Austin, August 2006.

where R_r is the resistance of the test structure measured at room temperature, ΔR is the resistance increase due to higher temperature, T is the temperature at which the test was conducted, and T_r is the room temperature.

Resistance increase with applied current was also measured. The oven was maintained at a constant temperature of 120 °C. The resistance of the test structure was measured using various current. The result is shown in Figure A.2. The following relationship was obtained from Figure A.2.

$$\frac{\Delta R}{R_0}=0.158\times i^{2.165} \tag{A.2}$$

where R_0 is the resistance of the test structure measured using the minimal current (50mA), ΔR is the resistance increase due to higher testing current, and i is the testing current in Amp.

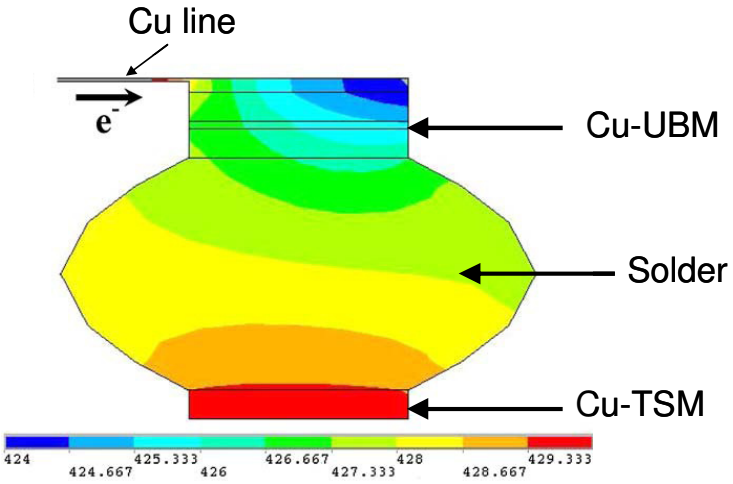


(Source: S. –H. Chae *et al*., in Ref [2.5])[12]

Figure A.2: Plot of the resistance increase with testing current

[12] With kind permission from S.-H. Chae, Master Report, the University of Texas at Austin, August 2006.

Equation (A.1) and (A.2) were obtained by measuring the overall resistance of the test structure. Therefore, the Joule heating effect of the Cu lines on the chip and on the substrates was also included. In order to obtain a more accurate estimate of the solder temperature, a finite element analysis (FEA) was conducted using ANSYS 9 to supplement the experimental results. Figure A.3 shows the simulated temperature gradient when the current was set to 1.01 Amp in the model. The length of the Cu line was adjusted in the model so that the applied current and the simulated quantities (overall resistance, and average temperature of the solder) satisfy both Equation (A.1) and (A.2). Under this condition, the solder temperature was found to be approximately 10 °C to 15 °C above the temperature measured at the backside of the Si chip in Chae's experiment (oven temperature of 140°C and current density of 4.12×10^4 Amp/cm^2 and 5.16×10^4 Amp/cm^2).



(Source: S. –H. Chae *et al*. in Ref [2.5])[13]

Figure A.3: Simulated temperature (in Kelvin) of the solder joint tested under a current of 1.01 Amp

[13] With kind permission from S.-H. Chae, Master Report, the University of Texas at Austin, August 2006.

Appendix B: Phase Composition Limits

This appendix describes the investigation of the pertinent Cu-Sn binary phase diagrams from which the composition limits were obtained in Table 3.1.

The composition limits of Cu, Cu_3Sn and Cu_6Sn_5 were obtained from the Cu-Sn binary phase diagram reported by Sanders and Miodownik [B.1], which is compiled in Alloy Phase Diagrams Center (online edition) by ASM International (Diagram No. 900891). At 150 °C, the composition limits of Cu were estimated to be 0.995 to 1 atomic fraction of Cu, the composition limits of Cu_3Sn were estimated to be 0.749 to 0.755 atomic fraction of Cu, and the composition limits of Cu_6Sn_5 were estimated to be 0.545 to 0.552 atomic fraction of Cu.

The Sn-rich side of the phase diagrams was estimated using the Cu-Sn binary phase diagram at Sn-rich compositions reported by Harding and Pell Walpole [B.2], which is compiled in Alloy Phase Diagrams Center (online edition) by ASM International (Diagram No. 906813). This phase diagram was plotted between 215°C and 315°C. This temperature range is above 150°C, the temperature of interest in this study. The composition limit of Cu in Sn at 150°C was estimated as follows.

(1) At 227°C, Sn phase composition limit is 0.00110 atomic fraction of Cu.

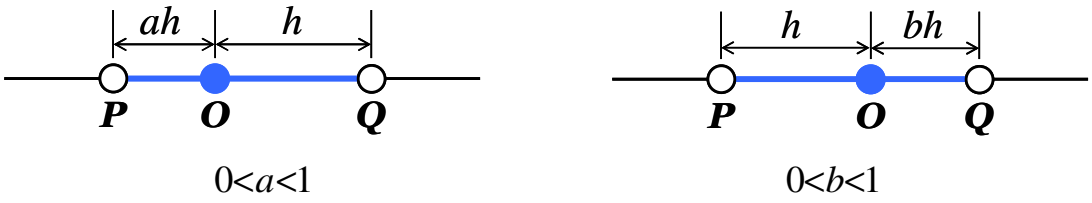
(2) At 215°C, Sn phase composition limit is 0.00102 atomic fraction of Cu.

Two estimations were made. The composition limit of Sn phase was first estimated to be 0.00059 atomic fraction of Cu at 150°C by extrapolation of (1) and (2). The composition limit of Sn phase could also be estimated to be 0.00102 if it was assumed that there is no significant change in composition limit between 150°C and

215°C. The second estimation was used in this study. The effect of the estimation of the composition limit of Sn phase on the model was limited to the fitting of Cu diffusivity in Sn phase and did not have any effect on the predicted phase growth kinetics once the parameter was fitted to the experimental observation.

Appendix C: Finite Difference in an Irregular Mesh

Incorporation of the moveable interface nodes leads to irregular meshing in the vicinity of the interfaces. Therefore, modification is required for the formulation of the finite difference of the first neighbors to the interface. As shown in Figure 3.6, the irregular meshing will affect the left and the right neighbors of the interface nodes. Figure C.1 shows three neighboring points O, P, and Q among which O is the point we will derive the finite difference for. In Figure C.1 (a), O and Q are in the regular mesh with spacing h whereas P has a reduced spacing ah. The result can be applied to the right neighbor of the interface node. In Figure C.1 (b), O and P are in the regular mesh with spacing h whereas Q has a reduced spacing bh. The result can be applied to the left neighbor of the interface node.



(a) (b)

Figure C.1: Mesh point O and neighbors P and Q in an irregular mesh. (a) O and right neighbor Q are on regular mesh points and left neighbor P is on an irregular mesh point. (a) O and left neighbor P are on regular mesh points and right neighbor Q is on an irregular mesh point.

Let $u(x,t)$ be a given function that is differentiable to its second partial derivative of x. In the neighborhood of $x=\bar{a}$, its second order approximation using Taylor series is the following.

$$u(x,t) \approx u(\bar{a}) + (x-\bar{a})\frac{\partial u}{\partial x} + \frac{1}{2}(x-\bar{a})^2 \frac{\partial^2 u}{\partial x^2} \tag{C.1}$$

To derive the finite difference of point O in Figure C.1 (a), one can simply take $\bar{a}=O$, into Equation (C.1), and apply it to $x=P$ and $x=Q$. This gives

$$u_P \approx u_O - ah\frac{\partial u_O}{\partial x} + \frac{1}{2}(ah)^2 \frac{\partial^2 u_O}{\partial x^2} \tag{C.2}$$

$$u_Q \approx u_O + h\frac{\partial u_O}{\partial x} + \frac{1}{2}h^2 \frac{\partial^2 u_O}{\partial x^2} \tag{C.3}$$

From Equations (C.2) and (C.3), $\frac{\partial^2 u}{\partial x^2}$ and $\frac{\partial u}{\partial x}$ can be solved algebraically to give

$$\frac{\partial^2 u_O}{\partial x^2} \approx \frac{2}{h^2}\left[\frac{1}{a(1+a)}u_P - \frac{1}{a}u_O + \frac{1}{1+a}u_Q\right] \tag{C.4}$$

$$\frac{\partial u_O}{\partial x} \approx \frac{1}{h}\left[-\frac{1}{a(1+a)}u_P + \frac{1-a}{a}u_O + \frac{a}{a+1}u_Q\right] \tag{C.5}$$

Equations (C.4) and (C.5) are the second and first x partial derivatives at point O in Figure C.1 (a). These two equations are applied to Equation (3.29) to address x derivatives of the right neighbors of the interface nodes.

One can also derive the first and second derivatives at point O in Figure C.1 (b) in similar fashion. The results are the following.

$$\frac{\partial^2 u_O}{\partial x^2} \approx \frac{2}{h^2}\left[\frac{1}{1+b}u_P - \frac{1}{b}u_O + \frac{1}{b(1+b)}u_Q\right] \tag{C.6}$$

$$\frac{\partial u_O}{\partial x} \approx \frac{1}{h}\left[-\frac{b}{1+b}u_P - \frac{1-b}{b}u_O + \frac{1}{b(1+b)}u_Q\right] \tag{C.7}$$

Equations (C.6) and (C.7) are applied to Equation (3.28) to address x derivatives of the left neighbors of the interface nodes.

Appendix D: Boundary Phases of the Finite Difference Model

The boundary phases in the layered structure of the solder stack are Cu under bump metallization and Sn solder. As indicated in Table 4.1, the diffusion coefficients in these boundary phases are many orders of magnitude apart and therefore require special treatments in the finite difference model. They are described as follows.

Cu-UBM

As indicated in Table 4.1, diffusion in Cu phase is many orders of magnitude slower than diffusion in other phases. First, the diffusion of Sn in Cu phase during thermal aging was considered. The diffusion coefficients of Sn in Cu phase at 150°C reported in literature were 3.89×10^{-23} m^2/sec [4.2] and 4.18×10^{-27} m^2/sec [4.5]. Cu_3Sn phase was first treated as the source of Sn atoms, and the characteristic length $\sqrt{Dt}$ of Sn diffusion in Cu phase was calculated. For 300 hours of diffusion, the characteristic lengths were 0.071 nm and 6.72 nm based on the two reported diffusion coefficients respectively. However, the lattice constant of Cu is only 0.36 nm.

In addition, the intermetallic compound growth was as high as 2.5 μm for Cu_3Sn and 5.4 μm for Cu_6Sn_5 in 300 hours, as reported by Siewert [D.1]. Equation (D.1) describes the conservation of Cu atoms during thermal aging:

$$C_{Cu}d_{Cu}\delta_{Cu}+C_{Cu_3Sn}d_{Cu_3Sn}\delta_{Cu_3Sn}+C_{Cu_6Sn_5}d_{Cu_6Sn_5}\delta_{Cu_6Sn_5}=0 \qquad \text{(D.1)}$$

where C is the composition in weight percent of Cu atoms, d is the density in g/c.c., and δ is the thickness change in nm. The dissolution of the Cu phase can be estimated as follows:

$$\delta_{Cu} = -\frac{C_{Cu_3Sn} d_{Cu_3Sn} \delta_{Cu_3Sn} + C_{Cu_6Sn_5} d_{Cu_6Sn_5} \delta_{Cu_6Sn_5}}{C_{Cu} d_{Cu}} \quad \text{(D.2)}$$

Table D.1 lists the values used in the calculation of Equation (D.2). Therefore the Cu dissolution for 300 hours thermal aging was estimated to be 3574 nm, which is significantly greater than the Sn atom diffusion length estimated earlier.

Table D.1: Values used in Equation (D.2): The composition in weight percent of Cu was converted from the composition in atomic fraction reported in Table 3.1 using the atomic weight of Cu (63.546 [D.2]) and Sn (118.71 [D.2])

	C (wt % Cu)	d (g/c.c.)	δ (nm)
Cu	100%	8.96 [D.3]	
Cu_3Sn	61.9%	9.00 [D.4]	+2546 [D.1]
Cu_6Sn_5	39.4%	8.37 [D.4]	+5388 [D.1]

These analyses indicate that Sn atoms barely diffused into the Cu under bump metallization during thermal aging. Under current stressing, the electromigration driving force further suppressed the diffusion of Sn atoms into Cu phase. Therefore, Cu under bump metallization was treated as a dissolving phase in the model. The composition of the Cu under bump metallization was assumed to be pure Cu with the exception of the Cu/Cu_3Sn interface where the composition was the solubility limit of Sn atom in Cu phase. In addition, the chemical diffusion of Sn in Cu phase was considered negligible.

Sn Solder

The diffusion coefficient of Cu atom in Sn solder is many orders of magnitude higher than those in the other phases. Additional simulation of the diffusion in Sn phase only was conducted using fixed interfaces. The diffusion coefficient of Cu in Sn solder was 1.5×10^{-11} m^2/sec, which was the same value to generate the simulation results presented in Chapter 5. Figure D.1 shows the closed form solution of Cu diffusion in Sn as a semi-infinite phase. Figure D.2 shows the finite difference solution when the solder was subjected to 5×10^4 Amp/cm^2 current stressing. Figures D.1 and D.2 indicate that the Sn solder is saturated with Cu atoms within very short period of time due to the rapid Cu diffusion. Therefore, the Sn solder was treated as a phase saturated with Cu atoms in the model presented in this dissertation.

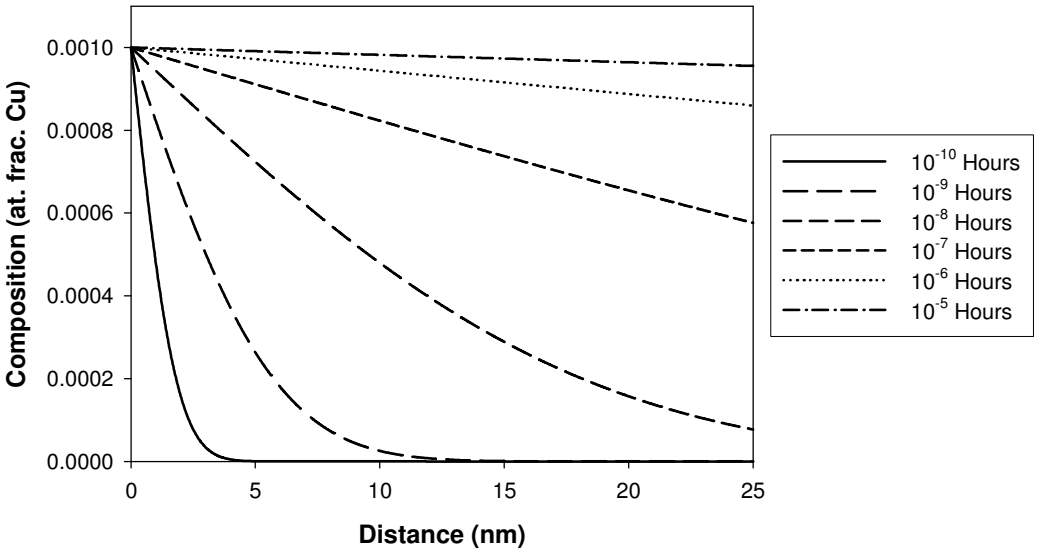


Figure D.1: Composition profiles for diffusion of Cu atoms into Sn solder during thermal aging; Sn was treated as a semi-infinite phase with composition of pure Sn at $x = \infty$

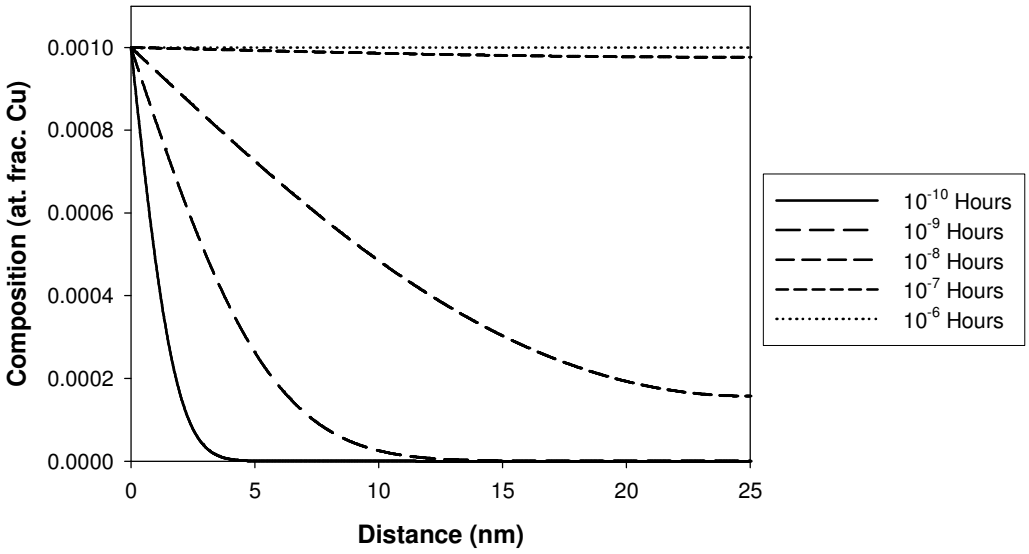


Figure D.2: Composition profiles for diffusion of Cu atoms into Sn solder during 5.16×10^4 Amp/cm^2 current stressing with the boundary condition $\partial C/\partial x=0$ at x = 25 nm

Appendix E: Atomic Densities

The atomic densities were obtained by dividing the densities by the molecular weight. The atomic fractions of Cu in Cu_3Sn and Cu_6Sn_5 were assumed to be 0.752 and 0.549, the center points of their composition ranges, as reported in Table 3.1. The atomic weights of Cu and Sn are 63.55 and 118.7 (Source: WebElements [http://www.webelements.com/]). The atomic densities of Cu_3Sn and Cu_6Sn_5 are listed in Table E.1.

Table E.1: The atomic densities of Cu_3Sn and Cu_6Sn_5

Phase	Cu_3Sn	Cu_6Sn_5
Density (g/cm^3)	8.9 [E.1]	8.28 [E.1]
Molecular weight (g/mol)	77.22	88.42
Atomic density (mol/cm^3)	0.115	0.094

For Cu and Sn, the molar volumes are 7.11 cm^3/mol and 16.29 cm^3/mol (Source: WebElements [http://www.webelements.com/]). Therefore, the atomic densities of Cu and Sn are 0.141 mol/cm^3 and 0.061 mol/cm^3 respectively.

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Vita

Huang-Lin Chao was born in Taipei, Taiwan, Republic of China, on December 31, 1973, the son of En-Po Chao and Chin Chueh. After graduating from the Affiliated High School of National Taiwan Normal University, Taipei, Taiwan in 1992, he entered the National Chiao Tung University, Hsinchu, Taiwan. He received the degree of Bachelor of Science in Mechanical Engineering in June 1996. In September 1996, he entered the Graduate School of the National Tsing Hua University, Hsinchu, Taiwan, in the Department of Power Mechanical Engineering. He conducted research in contact stress analysis of conjugated cams using photoelastic methods under the supervision of Professor Wei-Chung Wang. He received the degree of Master of Science and Engineering in June 1998. He served two years in the Republic of China Air Force in secretarial positions and was stationed in various air base and locations. After the honorable discharge in 2000, he worked for Applied Materials, Inc. in Taiwan as a Customer Engineer for two years. His expertise includes Physical Vapor Deposition (PVD) of various metallization materials in the Back End Of the Line (BEOL) technology, and his clients included the engineers in the 200 mm facilities of United Microelectronics Corporation (UMC) in Hsinchu, Taiwan. In August 2003, he began the doctoral program in Mechanical Engineering at the University of Texas at Austin, Austin TX. He joined the research group of Professor Paul S. Ho in Mechanical Engineering in June 2004. Under Professor Ho's supervision, he conducted research in solder electromigration and various topics such as dielectric, and viscoelastic behaviors of materials. In June 2005, he also joined the research group of Professor C. Grant Willson in Chemical Engineering. Under Professor Willson's supervision, he conducted

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